iC-NQE

16-bit Sin/D CONVERTER WITH SIGNAL CALIBRATION

preliminary

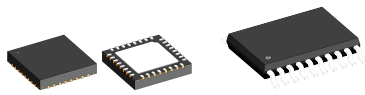
FEATURES

- Resolution of up to 16384 angle steps per sine period
- Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
- Count-safe vector follower principle, real-time system with 80 MHz sampling rate
- Direct sensor connection; selectable input gain
- Rail-to-rail input (frequency of up to 500 kHz)
- Calibration for offset, amplitude, phase and distortion
- A/B quadrature signals of up to 10 MHz with adjustable minimum transition distance
- Up to 32 bit period counting with zero processing or absolute data interface
- Absolute angle output via fast serial interface (BiSS, SSI, SPI)
- Permanent bidirectional memory access to parameters and OEM data by BiSS C
- Error monitoring of frequency, amplitude and configuration
- Device setup from serial EEPROM or using serial interface
- Single 3.3 V or 5 V supply
- ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

- Interpolator IC for angle resolution from sine/cosine sensor signals
- Optical encoders
- MR sensor systems

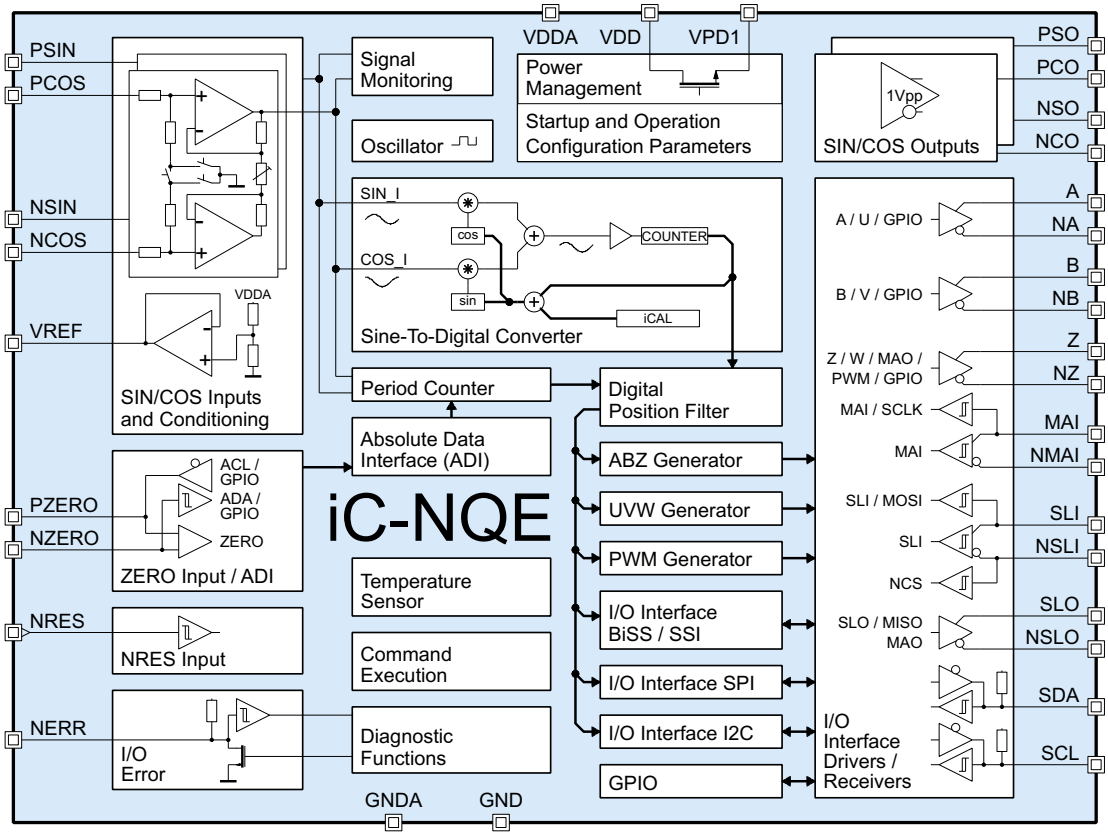
PACKAGES



QFN32
5 mm x 5 mm
RoHS compliant

TSSOP20
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-NQE is a next-generation monolithic A/D converter that uses the count-safe vector follower principle to convert sine/cosine sensor signals into angular position data with selectable resolution and hysteresis.

The analog front-end (AFE) features precision instrumentation amplifiers with differential inputs, permitting sensor bridges to be directly connected without the need for external resistors. The input gain is gradually adjustable and is suitable for both complementary sensor signals from about 20 mVpp to 1.5 Vpp and non-complementary single-sided sensor signals from about 40 mVpp to 3 Vpp.

Several programmable D/A converters are available for analog correction of signal errors with respect to offset, sin/cos amplitude matching, and phase: two 12-bit DACs for offset compensation, one 12-bit DAC for gain ratio, and one 10-bit DAC for phase compensation. In addition, if necessary, the transfer function of the sine-to-digital converter can be adjusted if signal distortions have to be compensated.

The interpolated angle is output as absolute data via the bidirectional, synchronous-serial I/O interface in BiSS C protocol allowing data rates of up to 10 Mbit/s. Alternatively, a Gray or binary coded SSI output format can be selected, with or without error bits. SSI ring mode is also supported to increase safety by redundant transmissions.

The sin/cos input cycles are tracked by a fast 32-bit period counter additionally, allowing to supplement the output data by a multiturn position.

At the same time, the angle changes are converted into incremental quadrature signals, maintaining a preset minimum transition distance between A and B. This allows adaptation to the respective system, for reliable cable transmission and without overriding the external quadrature counter. If an index sensor releases the zero inputs PZERO and NZERO, a synchronized index signal is available at the Z output, adjustable in its position and gating with AB.

Alternatively, the zero inputs can be operated as Absolute Data Interface (ADI) to process BiSS or SSI data of a multiturn sensor. In this way, the internal counters can be initialized and periodically checked.

iC-NQE offers various interfaces for configuration: an I^2C master interface to boot from an external EEPROM (with CRC verification), and an I^2C slave interface to connect a local MCU, and alternatively, the bidirectional register communication over BiSS C with the remote control (PLC). With a serial EEPROM connected, extra memory for OEM and USER data is available via BiSS.

Extended Features (offered with 32-pin QFN)

Additional I/O interface pins allow to output differential encoder quadrature signals with RS-422 compatibility for 120 Ω line termination, saving the line driver in typical 5 V applications. Alternatively, single-ended output of ABZ is supported along with adjustable UVW commutation signals for BLDC motor control.

In addition, the BiSS interface is supported by embedded RS-422 transceivers that enable robust data transmission through differential signals. A differential data input eases the daisy-chaining of multiple sensors without losing valuable board space.

Instead of using BiSS, the I/O interface pins can be assigned with SPI for fast communication with an embedded MCU.

Differential sine/cosine signals, conditioned and level stabilized, are additionally available via line drivers providing the 1 Vpp industry standard signal for PLC side termination with 100 Ohm.

General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

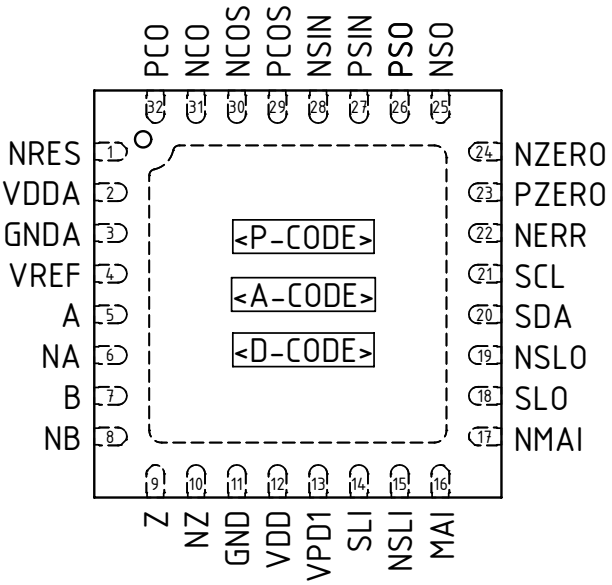
For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.

For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN32-5x5



PIN FUNCTIONS

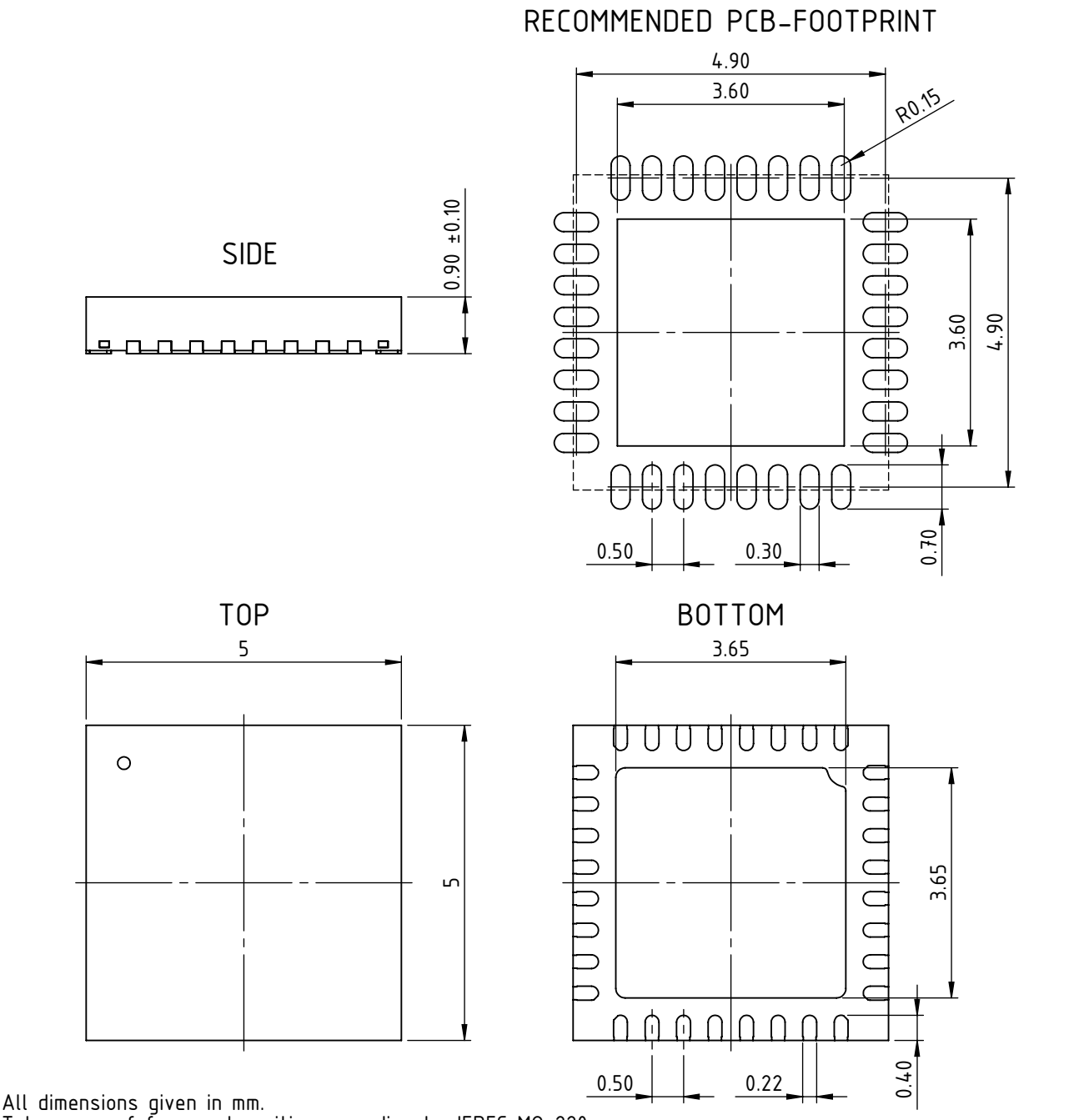
No.	Name	Function
1	NRES	Reset/Standby Input
2	VDDA [1]	+3.0 to 5.5 V Supply Voltage (analog)
3	GNDA [2]	Ground (analog)
4	VREF	Reference Voltage Output
5	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (calib.)
6	NA	Incremental Output NA
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (calib.)
8	NB	Incremental Output NB

PIN FUNCTIONS

No.	Name	Function
9	Z	Incremental Output Z PWM signal for Phase/Ratio (calib.)
10	NZ	Incremental Output NZ
11	GND	Ground
12	VDD	+3.0 to 5.5 V Supply Voltage (digital)
13	VPD1	Internal 1.8 V Logic Supply Voltage (do not wire)
14	SLI [3]	I/O Interface, data input + (SPI: MOSI)
15	NSLI	I/O Interface, data input - (SPI: NCS)
16	MAI	I/O Interface, clock line + (SPI: SCLK)
17	NMAI	I/O Interface, clock line -
18	SLO	I/O Interface, data output + (SPI: MISO)
19	NSLO	I/O Interface, data output -
20	SDA	I^2C Interface, data line Analog signal SIN+ (TMA mode)
21	SCL	I^2C Interface, clock line Analog signal SIN- (TMA mode)
22	NERR	Error Input/Output, active low
23	PZERO	Input Zero Signal + (ADI: Clock Line ACL)
24	NZERO	Input Zero Signal - (ADI: Data Line ADA)
25	NSO	Output Sine -
26	PSO	Output Sine +
27	PSIN	Input Sine +
28	NSIN	Input Sine -
29	PCOS	Input Cosine +
30	NCOS	Input Cosine -
31	NCO	Output Cosine -
32	PCO	Output Cosine +
	BP [4]	Backside paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] A lower voltage at VDDA against VDD is not allowed. If applicable, an external Schottky diode is necessary.
[2] External connections linking GND to GNDA are required.
[3] If only a single iC-NQE is used and no chain circuitry of multiple BiSS slaves, pins SLI and NSLI can only remain unwired in single end configuration.
[4] Connecting the backside paddle is recommended by a single link to GNDA. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS : QFN32-5x5



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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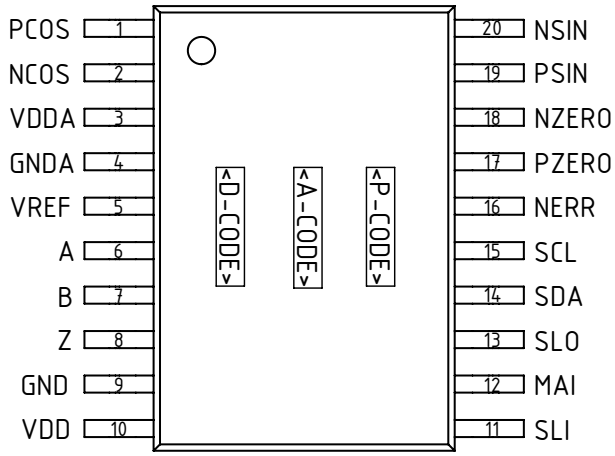
PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



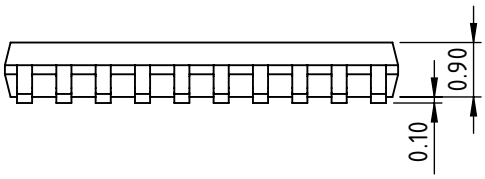
PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	VDDA [1]	+3.0 to 5.5 V Supply Voltage (analog)
4	GNDA [1]	Ground (analog)
5	VREF	Reference Voltage Output
6	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (calib.)
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (calib.)
8	Z	Incremental Output Z PWM signal for Phase/Ratio (calib.)
9	GND	Ground
10	VDD	+3.0 to 5.5 V Supply Voltage (digital)
11	SLI [2]	I/O Interface, data input
12	MAI	I/O Interface, clock line
13	SLO	I/O Interface, data output
14	SDA	I^2C Interface, data line Analog signal SIN+ (TMA mode)
15	SCL	I^2C Interface, clock line Analog signal SIN- (TMA mode)
16	NERR	Error Input/Output, active low
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

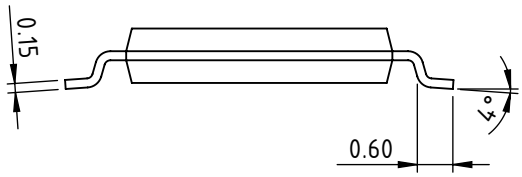
IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] External connections linking VDDA to VDD and GND to GNDA are required.
[2] If only a single iC-NQE is used and no chain circuitry of multiple BiSS slaves, pin SLI can remain unwired or can be linked to ground (GND).

PACKAGE DIMENSIONS : TSSOP20

SIDE



FRONT



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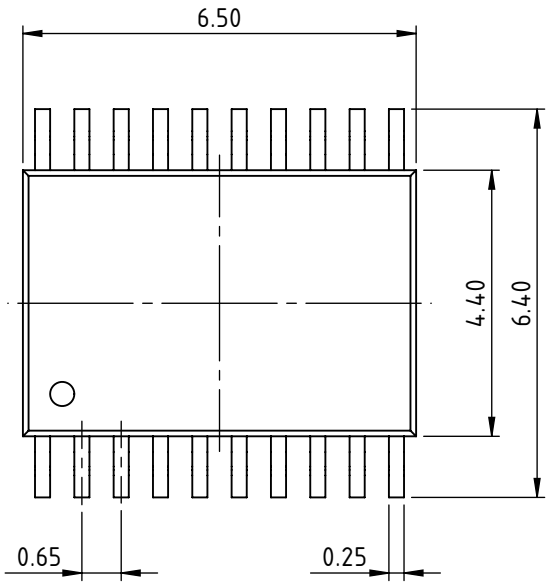
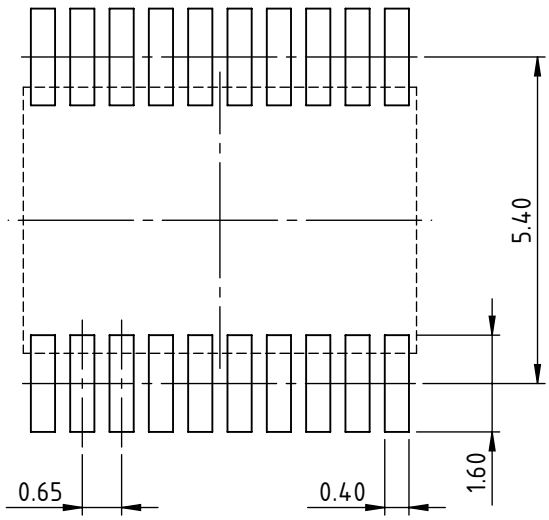


RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDDA)	Voltage at VDDA		-0.3	6	V
G002	I(VDDA)	Current in VDDA		-20	20 (tbd)	mA
G003	V(VDD)	Voltage at VDD	VDD < VDDA + 0.3 V	-0.3	6	V
G004	I(VDD)	Current in VDD		-20	20 (tbd)	mA
G005	V(VPD1)	Voltage at VPD1		-0.3	2 (tbd)	V
G006	I(VPD1)	Current in VPD1		-20	20 (tbd)	mA
G007	V(GND)	Voltage at GND		-0.3	0.3	V
G008	I(GND)	Current in GND		-20	20 (tbd)	mA
G009	Vpin()	Voltage at PSIN, NSIN, PCOS, NCOS, VREF, PSO, NSO, PCO, NCO	tbd (V() < VDDA + 0.3 V)	-0.3	6 (tbd)	V
G010	I()	Current in PSIN, NSIN, PCOS, NCOS, VREF, PSO, NSO, PCO, NCO		-20	20	mA
G011	Vpin()	Voltage at NRES, A, NA, B, NB, Z, NZ, SLO, NSLO, SDA, SCL, NERR, PZERO, NZERO		-0.3	6	V
G012	I()	Current in NRES, A, NA, B, NB, Z, NZ, SLO, NSLO, SDA, SCL, NERR, PZERO, NZERO		-20	20	mA
G013	Vpin()	Voltage at MAI, NMAI, SLI, NSLI		-10	10	V
G014	I()	Current in MAI, NMAI, SLI, NSLI		-100	100 (tbd)	mA
G015	Ilu()	Pulse Current in all pins (Latch-up Strength)	according to Jedec Standard No. 78; Ta = 25 °C, pulse duration to 10 ms, VDDA = $VDDA_{max}$, VDD = VDD_{max}, Vlu() = (-0.5...+1.5) x $Vpin()_{max}$	-100	100	mA
G016	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G017	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package TSSOP20 package QFN32-5x5	-20 -40		85 125	°C °C
T02	Rthja	Thermal Resistance Chip to Ambient	package TSSOP20 package QFN32-5x5, surface mounted to PCB according to JEDEC 51		80 40		K/W K/W
T03	Ts	Storage Temperature	package TSSOP20, QFN32-5x5	-40		140	°C

All voltages are referenced to pin GNDA unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods.							
001	V(VDDA)	Permissible Supply Voltage		3.0 4.5		3.6 5.5	V V
002	V(VDD)	Permissible Supply Voltage	V(VDD) ≤ V(VDDA)	3.0 4.5		3.6 5.5	V V
003	I(VDDA)	Supply Current in VDDA	NRES = 1, fin() = 250 kHz; A, B, Z open NRES = 0			15 0.1	mA mA
004	I(VDD)	Supply Current in VDD	NRES = 1, fin() = 250 kHz; A, B, Z open NRES = 0			20 0.1	mA mA
005	Vc()hi	Clamp Voltage hi at MAI, NMAI, SLI, NSLI	I() = 1 mA, other pins open	10		18	V
006	Vc()hi	Clamp Voltage hi at PZERO, PSIN, PCOS, NZERO, NSIN, NCOS, VREF, PSO, NSO, PCO, NCO	Vc()hi = V() - V(VDDA); I() = 1 mA, other pins open	0.4		2.2	V
007	Vc()hi	Clamp Voltage hi at SDA, SCL, NERR, SLO, A, B, Z, NA, NB, NZ, NSLO, NRES	Vc()hi = V() - V(VDD); I() = 1 mA, other pins open	0.4		2.2	V
008	Vc()lo	Clamp Voltage lo at MAI, NMAI, SLI, NSLI	I() = -1 mA, other pins open	-20		-10	V
009	Vc()lo	Clamp Voltage lo at all pins (with exception MAI, NMAI, SLI, NSLI)	I() = -1 mA, other pins open	-1.6		-0.2	V
Startup and Operation							
101	fosc	Oscillator Frequency	presented at pin SCL with subdivision of 320	73	80	85	MHz
102	TCosc	Oscillator Frequency Temperature Drift			-0.04		%/K
103	tbusy()cfg	Duration of Startup Configuration	SDA = 0 No EEPROM connected Undisturbed EEPROM access, ICAL_EN = 0 Undisturbed EEPROM access, ICAL_EN = 1		1.25 40 17.5 360		ms ms ms ms
Power Management: NRES, VPD1							
201	Vt()hi	Input Threshold Voltage hi at NRES				2	V
202	Vt()lo	Input Threshold Voltage lo at NRES		0.8			V
203	Vt()hys	Input Hysteresis at NRES	Vt()hys = Vt()hi − Vt()lo	120			mV
204	VDDAon	VDDA On Monitoring Threshold	presented at VDDA_OK VDDA_BOT = 0 or at Power-On VDDA_BOT = 1	 2.8 4.2		 2.97 4.5	 V V
205	VDDAoff	VDDA Off Monitoring Threshold	presented at VDDA_OK VDDA_BOT = 0 or at Power-On VDDA_BOT = 1	 2.62 4.05		 2.85 4.35	 V V
206	VDDAhys	VDDA Monitoring Hysteresis	VDDAhys = VDDAon − VDDAoff	150			mV
207	VDDon	VDD On Monitoring Threshold	presented at VDD_OK VDD_BOT = 0 or at Power-On VDD_BOT = 1	 2.8 4.2		 2.97 4.5	 V V
208	VDDoff	VDD Off Monitoring Threshold	presented at VDD_OK VDD_BOT = 0 or at Power-On VDD_BOT = 1	 2.62 4.05		 2.85 4.35	 V V
209	VDDhys	VDD Monitoring Hysteresis	VDDhys = VDDon − VDDoff	150			mV
210	VPD1on	VPD1 Turn-On Threshold	presented at VPD1_OK (internal only!)	1.58	1.62	1.70	V
211	VPD1off	VPD1 Turn-Off Threshold (undervoltage reset)	presented at VPD1_OK (internal only!)	1.47	1.52	1.65	V
212	VPD1hys	VPD1 Hysteresis	VPD1hys = VPD1on − VPD1off	40	90		mV

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
213	VPD1	Digital Core Voltage	generated internally	1.62	1.8	1.98	V
214	VDDAdOn	VDDA On Voltage Domain Detection Threshold	presented at VDDA_DOM	3.75	3.85	4.00	V
215	VDDAdOff	VDDA Off Voltage Domain Detection Threshold	presented at VDDA_DOM	3.60	3.75	3.85	V
216	VDDAdHys	VDDA Off Voltage Domain Detection Hysteresis	VDDAdHys = VDDAdOn − VDDAdOff	130			mV
217	VDDdOn	VDD On Voltage Domain Detection Threshold	presented at VDD_DOM	4.20	4.30	4.45	V
218	VDDdOff	VDD Off Voltage Domain Detection Threshold	presented at VDD_DOM	3.80	3.90	4.05	V
219	VDDdHys	VDD Off Voltage Domain Detection Hysteresis	VDDdHys = VDDdOn − VDDdOff	380			mV
220	VBG	Bandgap Voltage	(internal only!)	1.28	1.33	1.38	V
Sin/Cos Inputs and Conditioning: PSIN, NSIN, PCOS, NCOS, VREF							
301	Vin()sig	Permissible Input Voltage	ISM = 0x0, 0x2, 0x3, see Fig. 18	0.4		VDDA − 0.6	V
			ISM = 0x4, see Fig. 19	0.32		VDDA − 0.64	V
			ISM = 0x5, see Fig. 20	1.2		VDDA + 0.1	V
			ISM = 0x7, see Fig. 21	-0.1		VDDA + 0.1	V
302	Vos()	Input Offset Voltage	referred to side of input; G() ≥ 4 G() < 4	 -2 -7.5		 2 7.5	 mV mV
303	TCos	Input Offset Voltage Temperature Drift	see 302		±0.1		µV/K
304	Iin()	Input Current	V() = 0 V ... VDDA ISM = 0	-100		100	nA
305	Rin()	Input Resistance	Tj = 27 °C ISM = 0x3, 0x5 (vs. GNDA) ISM = 0x2, 0x4 (PSIN vs. NSIN, PCOS vs. NCOS) ISM = 0x7 (vs. VREF)	 250 500 250	 315 630 315	 380 760 380	 kΩ kΩ kΩ
306	TCRin	Temperature Coefficient Rin			-0.08		%/K
307	Vcore()	Recommended Internal Signal Level	V() = V(SIN_I), V(COS_I)		4		Vpp
308	G()	Selectable Gain Factors	G() = G(ISM) * GFx * GR fine gain GFx coarse gain GR	⅔ 1 2		96 12 8	
309	G(ISM)	Voltage Divider Gain	ISM = 0x0, 0x2, 0x3 ISM = 0x4, 0x5, 0x7		1 ⅓		
310	GA	Gain Accuracy	G() in accordance with tables GR, GFS, GFC and ISM	98		102	%
312	GFinl	Integral Linearity Error of Fine Gain	refer to fine gain GFS and GFC	-64		64	LSB
313	GFdnl	Differential Linearity Error of Fine Gain	refer to fine gain GFS and GFC	-1		3	LSB
314	VOScal	Offset Calibration Range	V(VDDA) = 3.3 V REFVOS = 0x0 REFVOS = 0x1 REFVOS = 0x3 V(VDDA) = 5.0 V REFVOS = 0x0 REFVOS = 0x1 REFVOS = 0x3	 ±980 ±980 ±640 ±980 ±1490 ±980	 ±1000 ±1000 ±660 ±1000 ±1515 ±1000	 ±1020 ±1020 ±680 ±1020 ±1540 ±1020	 mV mV mV mV mV mV
315	VOSinl	Integral Linearity Error of Offset Correction		-10		10	LSB

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
316	VOSdnl	Differential Linearity Error of Offset Correction		-1		1	LSB
317	PHcal	Phase Correction Range	sine vs. cosine signal PHMAX = 0x0 PHMAX = 0x1	 ±9 ±36	 ±11 ±40	 ±12 ±44	 DEG DEG
318	PHinl	Integral Linearity Error of Phase Correction		-10		10	LSB
319	PHdnl	Differential Error of Phase Correction		-1		1	LSB
320	fhc	Cut-off Frequency (-3 dB)	G() = 96, FCMP = 0x0 G() = 2, FCMP = 0x1		100 1000		kHz kHz
321	V(VREF)	Reference Voltage	I(VREF) = -1 mA ... +1 mA, DIS_VREF = 0	49		51	%VDDA
322	Vin(VREF)	Permissible Input Voltage at VREF	DIS_VREF = 1 V(VDDA) ≥ 4 V V(VDDA) < 4 V	 1.5 1.5		 VDDA − 2 VDDA − 1.5	 V V
323	Rin(VREF)	Input Resistance at VREF	DIS_VREF = 1 Rin() relative to Vin()cm Rin() relative to GNDA	 2.8 24			 kΩ kΩ
Sine-To-Digital Converter							
401	RESsdc	Converter Resolution			14		bit
402	AAabs	Absolute Angle Accuracy without calibration	referred to 360° input signal, see Fig. 2, HYS_CFG = 0, further conditions (tbd). input signal frequency (tbd)	-1.0 (tbd)		1.0 (tbd)	DEG
403	AAabs	Absolute Angle Accuracy after calibration	referred to 360° input signal, see Fig. 2, HYS_CFG = 0, further conditions (tbd). input signal frequency (tbd)	-0.5 (tbd)	±0.35	+0.5 (tbd)	DEG
404	AArel	Relative Angle Accuracy	referred to signal periods at A, resp. B (see Fig. 1); further conditions (tbd) FILT_EN = 0 FILT_EN = 1	 -10 (tbd) -2 (tbd)		 10 (tbd) 2 (tbd)	 % %
Zero Input and Absolute Data Interface: PZERO, NZERO							
501	Vos()	Input Offset Voltage	V() = Vcm(), EN_ZERO = 1	-6		6	mV
502	Ilk()	Input Leakage Current	EN_ZERO = 1 V() = 0.. VDD-0.4 V V() = VDD-0.4 V..VDDA	 -0.25 -0.25		 0.25 10	 uA uA
503	Vcm()	Common-Mode Input Voltage Range	EN_ZERO = 1	0.167		0.833	%VDDA
504	Vdm()	Differential Input Voltage Range	EN_ZERO = 1	0		VDD	V
505	Vt()hi	Input Threshold Voltage hi	EN_ZERO = 0			2	V
506	Vt()lo	Input Threshold Voltage lo	EN_ZERO = 0	0.8			V
509	Vt()hys	Input Threshold Hysteresis	Vt()hys = Vt()hi − Vt()lo	120			mV
510	Ipd(PZERO)	Input Pull-Down Current	V(PZERO) = 0.8 V..VDD, EN_ZERO = 0	10	22	50	µA
511	Ipu(NZERO)	Input Pull-Up Current	V(NZERO) = 0...VDD − 1 V, EN_ZERO = 0	-40	-22	-8	µA
512	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -4 mA, EN_ZERO = 0			390	mV
513	Vs()lo	Saturation Voltage lo	I() = -4 mA, EN_ZERO = 0			350	mV
514	tr()	Rise Time	V() = 10% → 90% VDD CL = 10 pF CL = 100 pF			 5 23	 ns ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
515	tf()	Fall Time	V() = 90% → 10% VDD CL = 10 pF CL = 100 pF			5 21	ns ns
Absolute Data Interface (ADI)							
601	f(ACL)	Clock Frequency at ACL	output at PZERO if ADI_EN = 1; ADI_CF = 0 (division of fosc / 534) ADI_CF = 1 (division of fosc / 54)		150 1500		kHz kHz
602	t_{Cycle}(ACL)	Cycle Time of ADI Frames	output at PZERO if ADI_EN = 1; Startup and ADI_FSTP = 1 (division of fosc / 16000) Operation or ADI_FSTP = 0 (division of fosc / 120000)		0.2 1.5		ms ms
Signal Monitoring (measured at SIN_I and COS_I, see Figures 1 and 16)							
701	Vpp()minE	Lower diff. Amplitude Threshold for Error-Monitoring of Sin^2+Cos^2	presented at AMP_E_L AMPT_EW = 0x0, REFAMPL = 1 AMPT_EW = 0x1, REFAMPL = 1 AMPT_EW = 0x2, REFAMPL = 1 AMPT_EW = 0x3, REFAMPL = 1 AMPT_EW = 0x0, REFAMPL = 0 AMPT_EW = 0x1, REFAMPL = 0 AMPT_EW = 0x2, REFAMPL = 0 AMPT_EW = 0x3, REFAMPL = 0	 tbd tbd tbd tbd tbd tbd tbd tbd	 1.05 1.45 2.05 2.60 39.8 54.9 77.7 98.5	 tbd tbd tbd tbd tbd tbd tbd tbd	 V V V V %VREF %VREF %VREF %VREF
702	Vpp()maxE	Upper diff. Amplitude Threshold for Error-Monitoring of Sin^2+Cos^2	presented at AMP_E_H REFAMPL = 1 REFAMPL = 0	 tbd tbd	 5.1 193.2	 tbd tbd	 V %VREF
703	Vpp()minW	Lower diff. Amplitude Threshold for Warning-Monitoring of Sin^2+Cos^2	presented at AMP_W_L AMPT_EW = 0x0, REFAMPL = 1 AMPT_EW = 0x1, REFAMPL = 1 AMPT_EW = 0x2, REFAMPL = 1 AMPT_EW = 0x3, REFAMPL = 1 AMPT_EW = 0x0, REFAMPL = 0 AMPT_EW = 0x1, REFAMPL = 0 AMPT_EW = 0x2, REFAMPL = 0 AMPT_EW = 0x3, REFAMPL = 0	 tbd tbd tbd tbd tbd tbd tbd tbd	 1.45 2.05 2.60 2.90 54.9 77.7 98.5 109.9	 tbd tbd tbd tbd tbd tbd tbd tbd	 V V V V %VREF %VREF %VREF %VREF
704	Vpp()maxW	Upper diff. Amplitude Threshold for Warning-Monitoring of Sin^2+Cos^2	presented at AMP_W_H REFAMPL = 1 REFAMPL = 0	 tbd tbd	 4.6 174.2	 tbd tbd	 V %VREF
705	Vpp()minG	Lower diff. Amplitude Threshold for Gain Control of Sin^2+Cos^2	presented at AMP_G_L AMPT_G_L = 0x5	 tbd	 3.85	 tbd	 V
706	Vpp()maxG	Upper diff. Amplitude Threshold for Gain Control of Sin^2+Cos^2	presented at AMP_G_H AMPT_G_H = 0x5	 tbd	 4.15	 tbd	 V
707	Vth()min	Threshold Voltage for Error Monitoring of Minimum Level	presented at AMP_E_M AMPT_EW = 0x0 AMPT_EW = 0x1 AMPT_EW = 0x2 AMPT_EW = 0x3	 53.0 55.0 56.0 57.0	 57.0 59.0 60.5 62.0	 61.0 63.0 65.0 67.0	 %VDDA %VDDA %VDDA %VDDA
Temperature Sensor							
801	TEMPres	Temperature Sensor Resolution			0.1		°C
802	TEMPrange	Temperature Sensor Range		-40		150	°C
803	TEMPacc	Temperature Sensor Accuracy				±3	°C
ABZ Generator: A, B, Z							
901	tminTD()	Minimum Transition Distance at A, B	refer to Figure 6 and Table 76 ABZ_MTD = 0x0		1 / fosc		
902	fmaxAB()	Maximum Frequency at A, B	refer to Figure 6 and Table 76 ABZ_MTD = 0x0		fosc / 4		

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PWM Generator: Z							
B01	fpwm()	PWM Frequency	derived from fosc with subdivision of 81920		0.977		kHz
B02	respwm()	PWM Resolution	derived from fosc		12.5		ns
I/O Interface BiSS / SSI							
C01	t_{P1}	Propagation Delay at SLO: SLO stable after MAI lo → hi		24	35	44	ns
C02	t_{P2}	Propagation Delay at SLO: SLO stable referenced to MAO lo → hi		-5		5	ns
C03	t_{TO}	Static BiSS Timeout at SLO	refer to Figure 9 BISS_TOS = 0x0 or 0x3 BISS_TOS = 0x1 BISS_TOS = 0x2	 19 1.4 121	 1600 / fosc 120 / fosc 10240 / fosc	 21.4 1.6 137	 µs µs µs µs µs µs
C04	t_{TOA}	Adaptive BiSS Timeout at SLO	refer to Figure 7; BISS_TOS = 0x3	(tbd)	t_{TOA_INIT} + 4/fosc	21.2	µs
C05	tbusy_r	Processing Time for Register Access	Undisturbed EEPROM access			250	µs
C06	tidle	Interface Blocking Time	powering up with no EEPROM			50	ms
I/O Interface SPI							
D01	t_{P4}	Propagation Delay at SLO: SLO stable after MAI hi → lo	PCFG_MAI = 0x0 (CMOS) or 0x1 (TTL) PCFG_SLO = 0x0 (SE)		20	tbd	ns
I/O Interface I2C							
E01	f(SCL)	Clock Frequency at SCL	derived from fosc with subdivision of 230		350		kHz
Sin/Cos Outputs: PSO, NSO, PCO, NCO							
F01	Vpk()max	Permissible Max. Output Amplitude	DC level = VDDA/2, RL = 50 Ω vs. VDDA/2			300	mV
F02	fc()out	Cut-off Frequency (-3 dB)	CL = 250 pF	500			kHz
F03	Voffs()	Offset Voltage		-100		+100	µV
F04	Isc()hi	Short-circuit Current hi	V() = 0 V	-25		-10	mA
F05	Isc()lo	Short-circuit Current lo	V() = VDD	10		25	mA
F06	SR()	Slew Rate	RLdiff = 100 Ω, CL = 25 pF		5		V/µs
F07	Ilk()	Tristate Leakage Current	EN_ADRV = 0	-1		1	µA
F08	RL()cal	Permissible Test Signal Load	TMA2 = 1 or TSA2 = 1	10			MΩ
F09	fout()cal	Permissible Test Signal Output Frequency	TMA2 = 1 or TSA2 = 1, CL = 200 pF			tbd	kHz
I/O Interface Receivers: A, NA, B, NB, Z, NZ (PCFG_x = 0 (single-ended, x = A, B, Z))							
G001	Vt()hi	Input Threshold Voltage hi				2	V
G002	Vt()lo	Input Threshold Voltage lo		0.8			V
G005	Vt()hys	Input Threshold Hysteresis	Vt()hys = Vt()hi − Vt()lo	120			mV
G006	Ipd()	Pull-Down Current	V() = 0.8 V..VDD	8	22	50	µA
I/O Interface Drivers: A, NA, B, NB, Z, NZ, SLO, NSLO (PCFG_x = 0 (single-ended, x = A, B, Z, SLO))							
G007	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(); I() = -4.0 mA		330	390	mV
G008	Vs()lo	Saturation Voltage lo	I() = 4.0 mA		270	350	mV
G009	tr()	Rise Time	V() = 10% → 90% VDD CL = 10 pF CL = 100 pF			 5 23	 ns ns
G010	tf()	Fall Time	V() = 90% → 10% VDD CL = 10 pF CL = 100 pF			 5 21	 ns ns
G013	RL()cal	Permissible Test Signal Load at A, B	TMA1 = 1 or TSA1 = 1	see F08			

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 140 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
G014	fout()cal	Permissible Test Signal Output Frequency at A, B	TMA1 = 1 or TSA1 = 1		see F09		
I/O Interface Drivers: A, NA, B, NB, Z, NZ, SLO, NSLO (PCFG_x = 1 (RS422, x = A, B, Z, SLO))							
G016	Vdiff()	Differential Output Voltage at A / NA, B / NB, Z / NZ, SLO / NSLO	Vdiff(A) = V(A) − V(NA); R(A,NA) ≥ 98.8 Ω, applies for B / NB, Z / NZ, SLO / NSLO as well $Vdiff_0$() (steady state '0') $Vdiff_1$() (steady state '1')	 2		 -2	 V V
G017	Isc()hi	Short-circuit Current hi	V() = 0 V	-150	-45	-20	mA
G018	Isc()lo	Short-circuit Current lo	V() = VDD	20	90	150	mA
G019	Ilk()	Power-off Leakage Current	V() = -0.25..+6 V	-100		100	µA
I/O Interface Receivers: MAI, NMAI, SLI, NSLI (PCFG_x = 0x0 or PCFG_x = 0x1 (single-ended, x = MAI, SLI))							
G101	$Vt()hi_C$	Input Threshold Voltage hi	PCFG_x = 0x0 (CMOS)			70	%VDD
G102	$Vt()lo_C$	Input Threshold Voltage lo	PCFG_x = 0x0 (CMOS)	30			%VDD
G103	$Vt()hi_T$	Input Threshold Voltage hi	PCFG_x = 0x1 (TTL)			2	V
G104	$Vt()lo_T$	Input Threshold Voltage lo	PCFG_x = 0x1 (TTL)	0.8			V
G105	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300			mV
G106	Ipu()	Pull-up Current in MAI, NSLI	V() = 0 ... VDD − 1 V	-40	-20	-10	µA
G107	Ipd()	Pull-down Current in SLI, NMAI	V() = 1 ... VDD	10	20	40	µA
I/O Interface Receivers: MAI, NMAI, SLI, NSLI (PCFG_x = 0x2 (RS422, x = MAI, SLI))							
G108	Rin()	Input Resistance	measured against GND	4			kΩ
G109	Vin()	Permissible Input Voltage		-10		10	V
G110	Vdiff()	Permissible Differential Input Voltage	Vdiff(MAI) = V(MAI) − V(NMAI), Vdiff(SLI) = V(SLI) − V(NSLI)	-12		12	V
G111	Vcm()	Permissible Input Common Mode Voltage		-7		7	V
G112	Vt()diff	Differential Input Threshold	Vt(MAI)diff = V(MAI) − V(NMAI), Vt(SLI)diff = V(SLI) − V(NSLI) Data signaling rate < 1 Mbit/s Data signaling rate 1 Mbit/s ... 5 Mbit/s Data signaling rate 5 Mbit/s ... 25 Mbit/s*	 -200 tbd. tbd.		 200 tbd. tbd.	 mV mV mV
G113	Vt()hys	Differential Input Hysteresis	$Vt(MAI)hys = Vt(MAI)diff_1 - Vt(MAI)diff_0$, $Vt(SLI)hys = Vt(SLI)diff_1 - Vt(MAI)diff_0$	10	80	200	mV
I/O Interface Drivers, Receivers and I/O Error: SDA, SCL, NERR							
G201	Vt()hi	Input Threshold Voltage hi				2	V
G202	Vt()lo	Input Threshold Voltage lo		0.8			V
G205	Vt()hys	Input Threshold Hysteresis	Vt()hys = Vt()hi − Vt()lo	120			mV
G206	Ipu()	Pull-Up Current	V() = 0..VDD − 1 V	-500		-170	µA
G207	Vs()lo	Saturation Voltage lo	I() = 4.0 mA		270	350	mV
G208	tf()	Fall Time	V() = 90% → 10% VDD, CL() = 100 pF	90		365	ns
G209	RL()cal	Permissible Test Signal Load at SDA, SCL	TMA1 = 1 or TSA1 = 1		see F08		
G210	fout()cal	Permissible Test Signal Output Frequency at SDA, SCL	TMA1 = 1 or TSA1 = 1		see F09		

* A 10 MHz clock signal has a data signaling rate of 20 Mbit/s

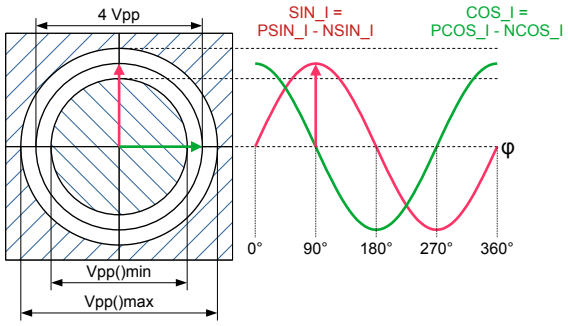

Figure 1: Differential amplitude thresholds for maximum and minimum monitoring.

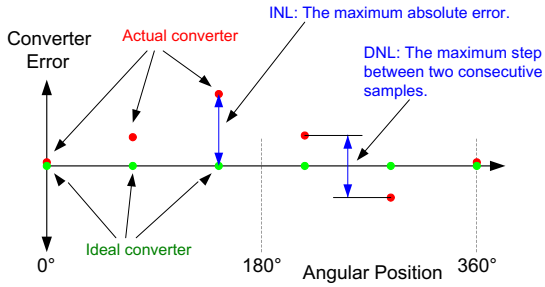

Figure 2: Integral and differential nonlinearity.

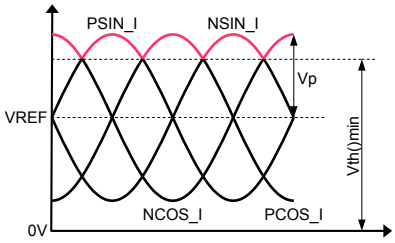

Figure 3: Threshold voltages for minimum level monitoring.

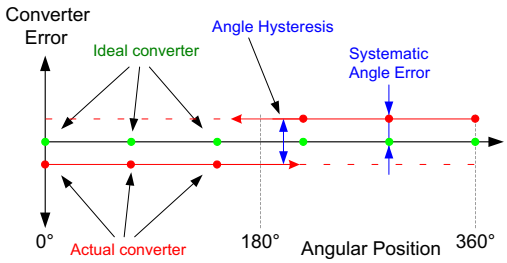

Figure 4: Systematic angle error due to hysteresis.

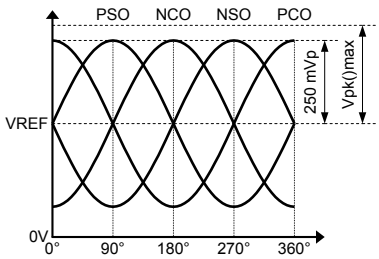

Figure 5: Output amplitude.

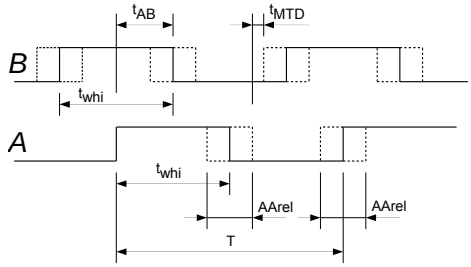

Figure 6: Relative angle error and minimum edge distance.

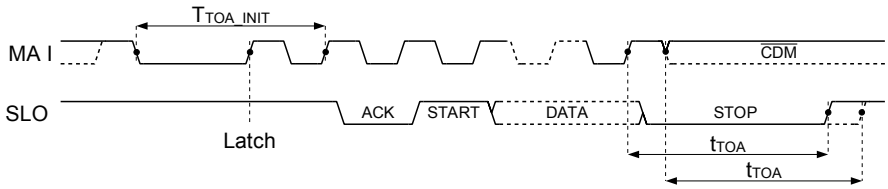

Figure 7: Adaptive BiSS timeout

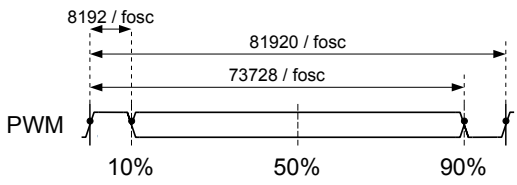

Figure 8: PWM timing

OPERATING REQUIREMENTS: BiSS / SSI Interface

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS/SSI						
I001	$1 / t_C$	Permissible Clock Frequency	BISS_VER < 2 (BiSS protocol) BISS_VER = 2 (SSI protocol)		12.5 4	MHz MHz
I002	t_{L1}	Clock signal high level duration	MAI = "1"	40	t_{TO}	ns
I003	t_{L2}	Clock signal low level duration	MAI = "0"	40	t_{TO}	ns
I004	t_{TO}	Static *BiSS* timeout	BISS_TOS < 3	see Elec. Char. C03		
I005	t_{TOA}	Adaptive *BiSS* timeout	BISS_TOS = 3, T_{CLK} = 20 ns	t_{TOA_INIT}	t_{TOA_INIT} + $3 \cdot T_{CLK}$	
I006	t_{P1}	Propagation Delay at SLO	For point-to-point configurations, referenced to rising edge of MAI	see Elec. Char. C01		
I007	t_{P2}	Propagation Delay at SLO	For bus configurations, referenced to rising edge of MAO	see Elec. Char. C02		
I008	t_{S1}	Setup Time: SLI stable before MA hi → lo		25		ns
I009	t_{H1}	Hold Time: SLI stable after MA hi → lo		25		ns
I010	t_{busy}	Processing time for single-cycle data	refer to Figure 9	$2 \cdot t_C$		
I011	t_{Cycle}	Permissible cycle time	No restrictions	*	indefinite	

Note: * Allow t_{TO} to elapse.

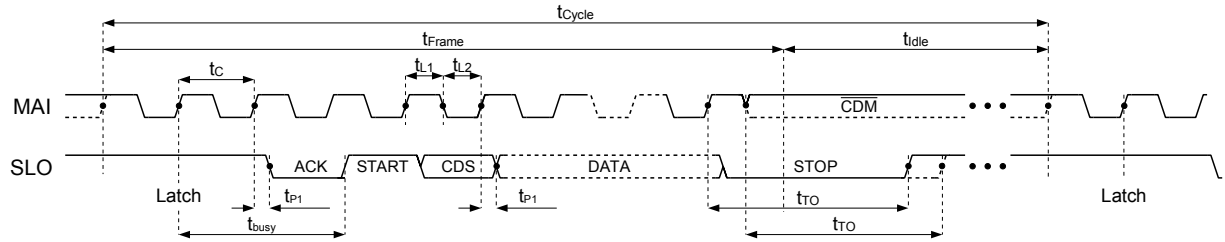

Figure 9: BiSS timing for point-to-point configuration (SLI = 0)

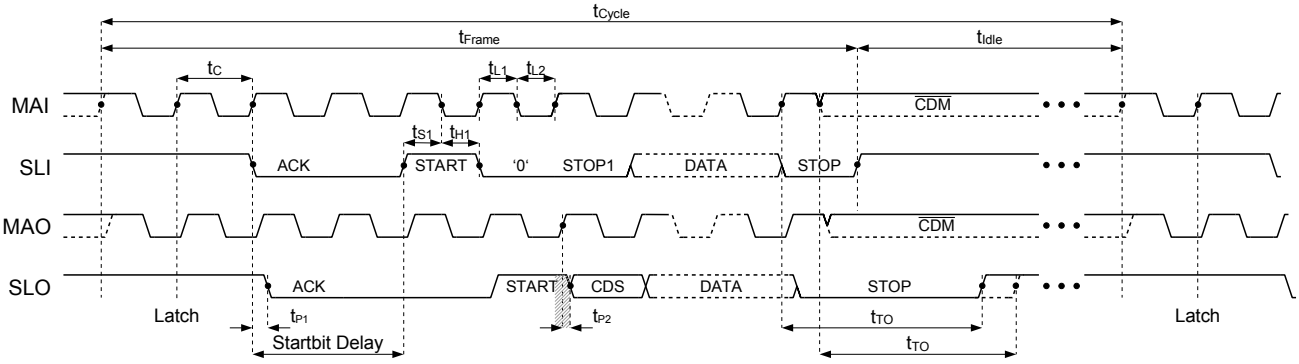

Figure 10: BiSS timing for bus configuration

OPERATING REQUIREMENTS: SPI

Operating Conditions: VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 125 °C, unless otherwise stated.
PCFG_x = 0x0 or PCFG_x = 0x1 (single-ended, x = MAI, SLI)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI						
I101	$1/t_{C1}$	Permissible Clock Frequency			10	MHz
I102	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo		800		ns
I103	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		100		ns
I104	t_{P1}	Propagation Delay: MISO stable after NCS hi → lo			50	ns
I105	t_{P2}	Propagation Delay: MISO high impedance after NCS lo → hi			50	ns
I106	t_{H1}	Hold Time: NCS lo after SCLK lo → hi	valid for SPI mode 3	30		ns
I107	t_{H3}	Hold Time: NCS lo after SCLK hi → lo	valid for SPI mode 0	50		ns
I108	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		tbd		ns
I109	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		tbd		ns
I110	t_{P3}	Propagation Delay: MISO stable after MOSI change	mode: repeating MOSI on MISO		tbd	ns
I111	t_{P4}	Propagation Delay: MISO stable after SCLK hi → lo	mode: sending data MISO	see Elec. Char. D01		
I112	t_{L1}	Clock Signal lo Level Duration		40		ns
I113	t_{L2}	Clock Signal hi Level Duration		40		ns

Note: NCS, SCLK, MOSI and MISO correlates to NSLI, MAI, SLI and SLO.

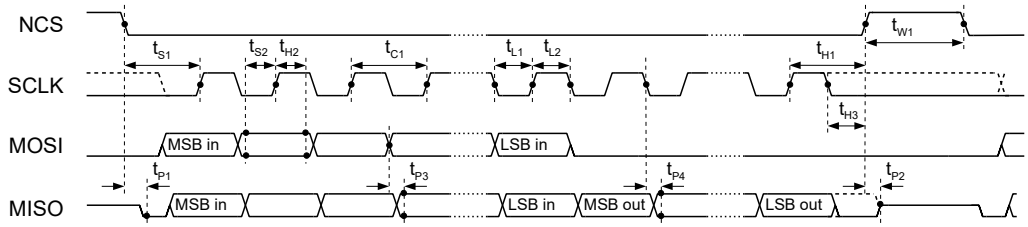

Figure 11: I/O Interface timing with SPI protocol

OPERATING REQUIREMENTS: Absolute Data Interface (ADI)

Operating Conditions: VDDA, VDD = 3.0...3.6 V or 4.5...5.5 V, VDDA ≥ VDD, GNDA = GND = 0 V, Tj = -40 ... 125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
ADI						
I201	$1/t_C$	Clock Frequency	refer to Elec. Char. No. 601 ADI_CF = 0 ADI_CF = 1	 135 1300	 155 1520	 kHz kHz
I202	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I203	t_S	Setup Time: Data stable before clock edge lo → hi		50		ns
I204	t_H	Hold Time: Data stable after clock edge lo → hi		10		ns
I205	t_{TO}	Permissible Slave Timeout		t_C	40	µs
I206	t_{Cycle}	Cycle Time	refers to Elec. Char. No. 602 Startup and ADI_FSTP = 1 Operation or ADI_FSTP = 0	 0.19 1.45	 0.22 1.63	 ms ms

Note: ACL and ADA correlates to the pins PZERO and NZERO (if ADI_EN = 1).

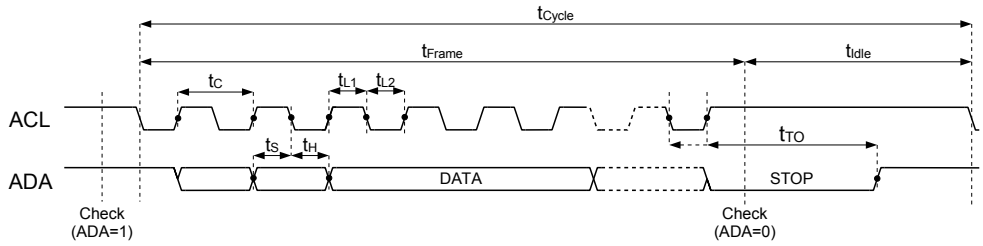

Figure 12: Absolute Data Interface (ADI)

CONFIGURATION PARAMETERS

REGISTER MAP

Configuration Parameters								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0								
Test Modes for Signal Calibration								
0x00	Reserved [0x00]						CALIB_EN(1:0)	
0x01	Reserved [0x00]							
0x02	TMA(7:0)							
0x03	TMA(15:8)							
0x04 ...0x0F	Reserved [0x00]							
Bank 1								
OTP								
0x00	SERNO(7:0)							
0x01 ...0x03	SERNO(31:8)							
0x04 ...0x0B	Reserved [Calibration Data]							
Bank 2								
I/O INTERFACE DRIVERS / RECEIVERS								
0x00	PCFG_Z	PCFG_B	PCFG_A	PCFG_SLO	PCFG_SLI(1:0)		PCFG_MAI(1:0)	
0x01	-	EN_PWM	EN_ZERO	EN_MAO	EN_UVW	EN_ABZ	EN_SPI	EN_BISS
SIN/COS OUTPUTS and TEMPERATURE SENSOR								
0x02	-	-	-	-	-	DIS_VREF	EN_TEMP	EN_ADRV
I/O INTERFACE I2C								
0x03	-	I2C_DEV0(6:0)						
0x04	-	I2C_DEV1(6:0)						
0x05	-	I2C_DEV2(6:0)						
0x06	-	I2C_DEV3(6:0)						
0x07	-	-	-	-	-	-	I2C_PAGE(1:0)	
I/O INTERFACE BiSS								
0x08	-	-	DL_PCR(5:0)					
0x09	-	-	-	-	STAT_CFG	BISS_ZB	BISS_VER(1:0)	
0x0A	BISS_DC3(1:0)		BISS_DC2	BISS_DC1	BISS_TOR(1:0)		BISS_TOS(1:0)	
0x0B	-	-	-	-	DL_IA(3:0)			
0x0C	CRC_INIT(5:0)						CRC_LC(1:0)	
I/O INTERFACE SSI and I/O INTERFACE SPI								
0x0D	-	-	-	SPI_LAT	-	SSI_STAT	SSI_RING	SSI_GRAY
0x0E	RPL_B2(1:0)		-	-	-	-	-	-
0x0F	CRC_B2(7:0)							
Bank 3								
SIN/COS INPUTS and CONDITIONING								
0x00	GR	PHMAX	REFVOS(1:0)		FCMP	ISM(2:0)		
0x01	GFS(3:0)				Reserved [0x0]			
0x02	GFS(11:4)							
0x03	GFC(3:0)				Reserved [0x0]			
0x04	GFC(11:4)							
0x05	OFS(3:0)				Reserved [0x0]			

Configuration Parameters								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	OFS(11:4)							
0x07	OFC(3:0)				Reserved [0x0]			
0x08	OFC(11:4)							
0x09	PH(2:0)			Reserved [0x00]				
0x0A	PH(10:3)							
SIGNAL MONITORING and AUTOMATIC GAIN CONTROL								
0x0B	GC_2CVAL	GC_2C	GC_I_GR	GC_EN	REFAMPL	Reserved [0]	AMPT_EW(1:0)	
0x0C	Reserved [0]	Reserved [0]	AMPT_G_L(2:0)			AMPT_G_H(2:0)		
POWER MANAGEMENT								
0x0D	-	-	-	-	-	-	VDD_BOT	VDDA_BOT
0x0E	RPL_B3(1:0)		-	-	-	-	-	-
0x0F	CRC_B3(7:0)							
Bank 4								
SINE-TO-DIGITAL CONVERTER								
0x00	-	FLEX_DIS	SUBDIV(1:0)		SELRES(3:0)			
0x01	-	-	ZERO_POS(1:0)		HYS_CFG(3:0)			
0x02	Reserved [0x4]				Reserved [1]	Reserved [0x1]		
0x03	-	CFGFILT(2:0)			ICAL_FAC(1:0)		ICAL_EN	FILT_EN
0x04	-	DIR	Reserved [0x1]		-	Reserved [1]	Reserved [0]	HYS_EN
0x05	Reserved [0x0]				Reserved [0x0]			
0x06	Reserved [0x00]							
0x07	-	Reserved [0x0]			-	-	Reserved [0x0]	
DIAGNOSTIC FUNCTIONS								
0x08	EM_FERR	EM_IA_C	EM_UVW	EM_ABZ	EM_ALPHA	EM_OMEGA	EM_IA_F	EM_ADI
0x09	ERR_LAT	EM_VDD	EM_VDDA	EM_EXT	EM_I2C	EM_AMPM	EM_AMPH	EM_AMPL
0x0A	WM_FERR	WM_IA_C	WM_UVW	WM_ABZ	WM_ALPHA	WM_OMEGA	WM_IA_F	WM_ADI
0x0B	WRN_LAT	WM_VDD	WM_VDDA	-	-	-	WM_AMPH	WM_AMPL
0x0C	RPL_B4(1:0)		-	-	-	-	-	-
0x0D	CRC_B4(7:0)							
Bank 5								
ZERO INPUTS and PERIOD COUNTER								
0x00	PCR_CBZ1	PCR_CBZ	PCR_TL(5:0)					
0x01	-	-	-	PCR_FC	PCR_ML(3:0)			
ABSOLUTE DATA INTERFACE (ADI)								
0x02	ADI_OFS(4:0)					ADI_SBL(2:0)		
0x03	ADI_DERR	ADI_PRIO	ADI_GRAY	ADI_DBP	ADI_WBL	ADI_EBL	ADI_CF	ADI_EN
0x04	ADI_RAW	ADI_DUAL	ADI_SWL(1:0)		ADI_CRC	ADI_BISS	ADI_GET	ADI_FSTP
0x05	-	-	-	ADI_GAP0(4:0)				
0x06	-	-	-	ADI_GAP1(4:0)				
0x07	RPL_B5(1:0)		-	-	-	-	-	-
0x08	CRC_B5(7:0)							
Bank 6								
ABZ GENERATOR								
0x00	ABZ_CPR(7:0)							
0x01	ABZ_CPR(15:8)							
0x02	-	-	ABZ_CPR(21:16)					

Configuration Parameters								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03	ABZ_ZLEN(1:0)		ABZ_ABPH(1:0)		ABZ_ZMSK	ABZ_STUP	ABZ_ZPOL	ABZ_DIR
0x04	-	-	ABZ_LAG(1:0)		ABZ_MTD(3:0)			
0x05	ABZ_OFFS(7:0)							
0x06 ...0x07	ABZ_OFFS(23:8)							
0x08	RPL_B6(1:0)		-	-	-	-	-	-
0x09	CRC_B6(7:0)							
Bank 7								
UVW GENERATOR								
0x00	-	-	-	UVW_CPR(4:0)				
0x01	-	-	-	-	-	-	UVW_POL	UVW_DIR
0x02	UVW_OFFS(7:0)							
0x03 ...0x04	UVW_OFFS(23:8)							
0x05	UVW_LTC(7:0)							
0x06	UVW_LTC(15:8)							
0x07	RPL_B7(1:0)		-	-	-	-	-	-
0x08	CRC_B7(7:0)							
Bank 8								
OUTPUT DATA								
0x00	IA_OFFS(7:0)							
0x01	IA_OFFS(15:8)							
0x02	PCR_OFFS(7:0)							
0x03 ...0x05	PCR_OFFS(31:8)							
0x06	RPL_B8(1:0)		-	-	-	-	-	-
0x07	CRC_B8(7:0)							
Bank 9								
MEMORY ORGANISATION								
0x00	RPL_BDOR	-	RPL_PRES(1:0)		RPL_B16_31(1:0)		RPL_B0(1:0)	
0x01	RPL_B35(1:0)		RPL_B34(1:0)		RPL_B33(1:0)		RPL_B32(1:0)	
0x02	RPL_B39(1:0)		RPL_B38(1:0)		RPL_B37(1:0)		RPL_B36(1:0)	
0x03	RPL_B43(1:0)		RPL_B42(1:0)		RPL_B41(1:0)		RPL_B40(1:0)	
0x04	RPL_B47(1:0)		RPL_B46(1:0)		RPL_B45(1:0)		RPL_B44(1:0)	
0x05	RPL_B51(1:0)		RPL_B50(1:0)		RPL_B49(1:0)		RPL_B48(1:0)	
0x06	RPL_B55(1:0)		RPL_B54(1:0)		RPL_B53(1:0)		RPL_B52(1:0)	
0x07	RPL_B59(1:0)		RPL_B58(1:0)		RPL_B57(1:0)		RPL_B56(1:0)	
0x08	RPL_B63(1:0)		RPL_B62(1:0)		RPL_B61(1:0)		RPL_B60(1:0)	
0x09	RPL_DEV3(1:0)		RPL_DEV2(1:0)		RPL_DEV1(1:0)		RPL_DEV0(1:0)	
COMMAND EXECUTION								
0x0A	-	-	-	CPL_BISS	CPL_F_IF	CPL_GPIO	CPL_PRES	CPL_F_EW
MEMORY ORGANISATION								
0x0B	CRC_ICAL(7:0)							
0x0C	CRC_ICAL(15:8)							
0x0D	RPL_B9(1:0)		-	-	-	-	-	-
0x0E	CRC_B9(7:0)							

Configuration Parameters								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SINE-TO-DIGITAL CONVERTER								
Bank 16								
0x00	iCAL[0](7:0)							
0x01 ...0x3F	iCAL[1:63](7:0)							
Bank 17 . . . 31								
0x00 ...0x3F	iCAL[64:1023](7:0)							
Notes								
Register marked with '-' are not implemented. They cannot be written to and are always read as '0'.								
Reserved [*]: Reserved registers must be programmed with the values provided in square brackets.								

Table 1: Configuration Parameters

Direct Access								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MEMORY ORGANISATION								
0x40	BSEL(7:0)							
BISS DEVICE INFO AND EDS								
0x41	EDS_BANK(7:0) [1]							
0x42	BP_ID(15:8) [1]							
0x43	BP_ID(7:0) [1]							
0x44	DEV_SN(31:24)							
0x45 ...0x47	DEV_SN(23:0)							
Preset Function								
0x48	PRES_IA(7:0)							
0x49	PRES_IA(15:8)							
0x4A	PRES_PCR(7:0)							
0x4B ...0x4D	PRES_PCR(31:8)							
0x4E	PRES_CRC(7:0)							
0x4F	-	-	-	-	-	-	-	-
OUTPUT DATA								
0x50	POS_IA(7:0)							
0x51	POS_IA(15:8)							
0x52	POS_PCR(7:0)							
0x53 ...0x55	POS_PCR(31:8)							
0x56	-	-	-	-	-	-	-	-
0x57	-	-	-	-	-	-	-	-
0x58	OMEGA(7:0)							
0x59 ...0x5A	OMEGA(23:8)							
0x5B ...0x5F	-	-	-	-	-	-	-	-
0x60	Reserved							
0x61	-	-	-	-	-	-	Reserved	
0x62	-	-	-	-	-	-	-	-
0x63	-	-	-	-	-	-	-	-
0x64	TEMP(7:0)							
0x65	TEMP(15:8)							
0x66	GC_GFS(7:0)							
0x67	-	-	-	GC_GR	GC_GFS(11:8)			
Status Flags								
0x68	UVW_OK	ABS_OK	RDY_CMD	RDY_UVW	RDY_ABZ	RDY_PHI	RDY_PCR	RDY_CFG
0x69	-	-	-	NERR_I	VDD_DOM	VDDA_DOM	VDD_OK	VDDA_OK
0x6A	-	AMP_E_M	AMP_E_H	AMP_E_L	AMP_W_H	AMP_W_L	AMP_G_H	AMP_G_L
0x6B	GC_ERR_H	GC_ERR_L	ZERO_OCC	STATE(4:0)				
Error Flags								
0x6C	ERR_FERR	ERR_IA_C	ERR_UVW	ERR_ABZ	ERR_ALPH	ERR_OMEG	ERR_IA_F	ERR_ADI
0x6D	ERR_FLAG	ERR_CFG	ERR_WD	ERR_EXT	ERR_I2C	ERR_AMPM	ERR_AMPH	ERR_AMPL
0x6E	-	I2C_ERC(2:0)		ADI_FRM(1:0)			ADI_PCR	ADI_EB
0x6F	-	-	-	-	-	-	ERR_VDD	ERR_VDDA

Direct Access								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Warning Flags								
0x70	WRN_FERR	WRN_IA_C	WRN_UVW	WRN_ABZ	WRN_ALPH	WRN_OMEG	WRN_IA_F	WRN_ADI
0x71	WRN_FLAG	-	-	-	-	-	WRN_AMPH	WRN_AMPL
0x72	-	-	-	-	-	-	-	-
0x73	-	-	-	-	-	-	WRN_VDD	WRN_VDDA
GPIO								
0x74	GPIO_D_7	GPIO_D_6	GPIO_D_5	GPIO_D_4	GPIO_D_3	GPIO_D_2	GPIO_D_1	GPIO_D_0
0x75	GPIO_F_7	GPIO_F_6	GPIO_F_5	GPIO_F_4	GPIO_F_3	GPIO_F_2	GPIO_F_1	GPIO_F_0
COMMAND EXECUTION								
0x76	CMD_STAT(7:0)							
0x77	CMD(7:0)							
BISS DEVICE INFO AND EDS								
0x78	DEV_ID(47:40) [1]							
0x79 ...0x7D	DEV_ID(39:0) [1]							
0x7E	MFR_ID(15:8)							
0x7F	MFR_ID(7:0)							
Notes								
Register marked with '-' are not implemented. They cannot be written to and are always read as '0'.								
[1] Content depends on addressed slave ID (BiSS C only)								

Table 2: Direct Access

STARTUP and OPERATION

After power up, iC-NQE monitors the voltages of the supply pins VDDA and VDD and starts generating the digital core voltage VPD1. All three voltages must be valid for operation until reading the internal one-time programmable memory (OTP) is executed, providing factory stored calibration data.

Subsequently, iC-NQE attempts to read the configuration data and, if enabled, the distortion correction data (iCAL) from the external EEPROM via the I^2C multi-master interface. If a properly configured EEPROM is present, the EEPROM contents including several checksums is transferred to RAM and the required CRCs executed. The error output NERR is active during this process (NERR = 0).

If no EEPROM is present or any CRC fails, two more EEPROM read attempts are executed. If the third and final attempt fails, the iC-NQE goes into error state and (NERR = 0).

In this case, the iC-NQE must be configured via any serial I/O interface (see sections I/O INTERFACE BiSS, I/O INTERFACE SPI and I/O INTERFACE I2C).

Reset values are defined for all parameters (see programming tables), which remain in the RAM until the appropriate CRC is passed.

If all CRCs are passed, the configuration data is considered valid and the converter starts operating; the error output is released to NERR = 1 (if no further error is detected).

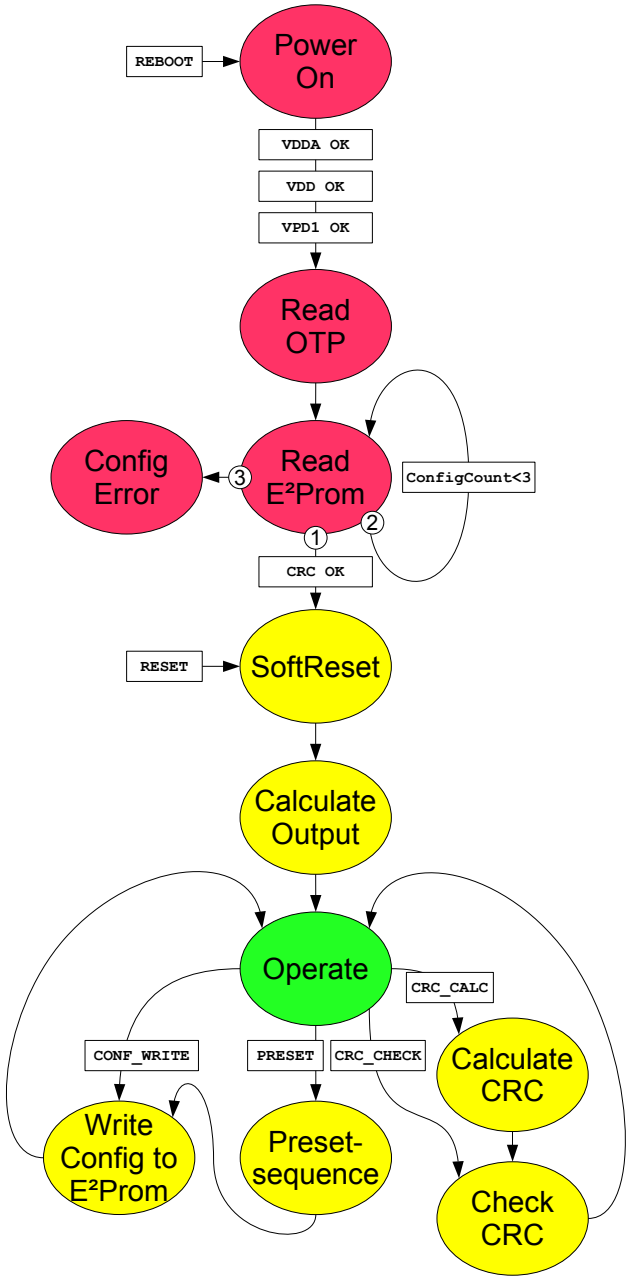

Figure 13: State Diagram

POWER MANAGEMENT

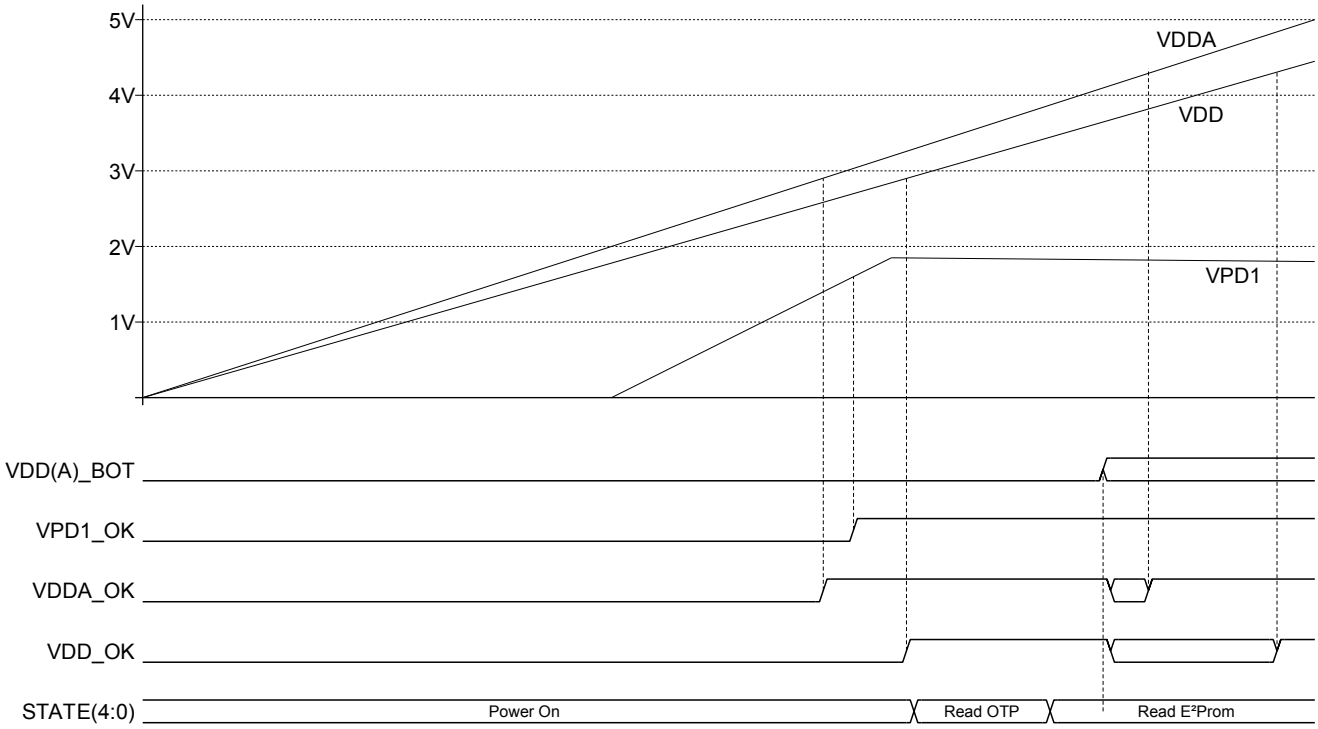

Figure 14: Startup Timing Diagram

When powering up, iC-NQE starts generating its VPD1 = 1.8 V core voltage at approximately 1.35 V, assuming the reset input NRES is at high level. The digital logic is kept in reset until VPD1_OK = 1 (see Elec. Char. No. 204, 207 and 210).

There are two more voltage monitoring circuits, one each per power supply pin, resulting in VDDA_OK and VDD_OK.

VDDA_OK	Addr. 0x69, bit 0	Read only
VDD_OK	Addr. 0x69, bit 1	Read only
Code	Function	
0	Voltage not ok	
1	Voltage ok	

Table 3: Voltage at VDD, VDDA OK

Both monitoring thresholds are programmable independently by VDDA_BOT and VDD_BOT (see Table 4). However, at startup both thresholds are set to 3 V by default (i.e. VDDA_BOT = 0 and VDD_BOT = 0 are the initial values). Refer 204 and 207 for further information on monitoring thresholds.

VDDA_BOT	Bank 0x3, Addr. 0x0D, bit 0	Reset: 0
VDD_BOT	Bank 0x3, Addr. 0x0D, bit 1	Reset: 0
Code	Function	
0	3.3V Brownout Threshold	
1	5V Brownout Threshold	

Table 4: Error: Missing text

If all three voltage monitoring circuits indicate OK, iC-NQE reads its OTP. If this is successful, reading the EEPROM is started.

In this phase the configuration of VDDA_BOT or VDD_BOT can change, so that the monitoring circuits may follow to change VDDA_OK or VDD_OK to NOT OK, at least temporarily, until the applied supply exceeds the configured monitoring threshold (see Figure 14).

Basically, voltage monitoring is divided into two domains, VDD and VDDA, which are monitored independently of each other. A distinction is made between a 3.3 V or 5 V power supply and reported to VDDA_DOM and VDD_DOM.

VDDA_DOM	Addr. 0x69, bit 2	Read only
VDD_DOM	Addr. 0x69, bit 3	Read only

Code	Function
0	3.3 V domain detected
1	5 V domain detected

Table 5: Voltage domain detection at VDD, VDDA

Note: VDDA ≥ VDD must be ensured for proper operation, especially when iC-NQE is switched on.

Resetting the iC-NQE is possible either by undervoltage or pulling the reset pin low (NRES = 0 V).

Idle Mode

When pin NRES is pulled low, iC-NQE enters a low-power idle mode (see 004 and 003). In this case, VPD1 core voltage generation is disabled and all pins are set to tristate. A floating pin NRES must be avoided, there is no internal pull-up or pull-down.

Attention: Do not allow pin NRES floating.

SIN/COS INPUTS and CONDITIONING

Input Configuration

The input stages are designed as instrumentation amplifiers and thus directly suitable for differential input signals. Single-ended input signals can be processed by applying the reference voltage of the input signal to the negative inputs.

Figure 15 shows the sine channel's conditioning unit for PSIN_I; for NSIN_I a complementary circuit exists. The cosine channel's set-up is equivalent to that of the sine channel.

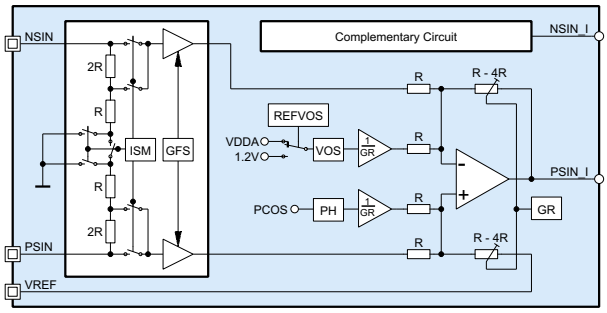

Figure 15: Signal-conditioning unit (sine channel)

Input Signal Mode

For high input amplitudes an optional voltage divider can be selected. This voltage divider reduces the amplitude of the input signal to 1/3 of the original value. Furthermore, the input impedance can be selected either differential to the inverted signal input or to the pin GNDA.

ISM(2:0)	Bank 0x3, Addr. 0x00, bit 2:0	Reset: 0x0
Code	Function	
0x0	Hi-Z Gain=1	
0x2	600k differential Gain=1	
0x3	300k to pin GNDA Gain=1	
0x4	600k differential Gain=0.33	
0x5	300k to pin GNDA Gain=0.33	
0x7	300k to pin VREF Gain=0.33	
Others	Not permitted	

Table 6: Input Signal Mode

Reference Voltage

The iC-NQE generates the reference voltage VREF, which is used for the signal conditioning (Figure 15), internally from VDDA/2. Since this reference voltage is output at pin VREF, the pin load must not exeed ±1 mA (see Elec.Char.321). If, however, an external reference voltage is preferred, the pin driver can be disabled with DIS_VREF and the external reference voltage can be applied to the VREF pin.

DIS_VREF	Bank 0x2, Addr. 0x02, bit 2	Reset: 0
Code	Function	
0	Internal VREF enabled	
1	Internal VREF disabled	

Table 7: Internal VREF Disable

Sine/Cosine Gain Settings

The total gain G() of the input amplifier is determined by the divider gain G(ISM), the coarse gain GR and the fine gains GFS or GFC.

Thus, the voltage gain G() between (*PSIN_I – NSIN_I*) and the inputs (*PSIN – NSIN*) is calculated as the product of G(ISM), G(GR) and G(GFS), or G(GFC) respectively.

The gain must be selected so that approximately the 1 Vpp-diff signal is output at PSO and NSO (i.e. a differential amplitude of 500 mV), or a 4 Vpp-diff signal at A and B (for TMA1 = 1). In addition, the cosine to sine amplitude matching must be carefully adjusted using the fine gain (GFC or GFS).

GR	Bank 0x3, Addr. 0x00, bit 7	Reset: 0
Code	Value	
0	2	
1	8	

Table 8: Coarse Gain Factor

GFS(3:0)	Bank 0x3, Addr. 0x01, bit 7:4	Reset: 0x0
GFS(11:4)	Bank 0x3, Addr. 0x02, bit 7:0	Reset: 0x00
GFC(3:0)	Bank 0x3, Addr. 0x03, bit 7:4	Reset: 0x0
GFC(11:4)	Bank 0x3, Addr. 0x04, bit 7:0	Reset: 0x00
Code	Value	
0x000	1.0	
...	$12.0^{(Code/4095)}$	
0xFFF	12.0	

Table 9: Fine Gain Factor Sine and Cosine

To improve amplifier stability and noise performance, the frequency compensation should be set to 'high' whenever the sine or cosine fine gains are below 0x800. If the input frequency remains sufficiently low, this frequency compensation setting can also be used at the higher gain values.

FCMP	Bank 0x3, Addr. 0x00, bit 3	Reset: 0
Code	Function	
0	Low	
1	High	

Table 10: Frequency Compensation

Sine/Cosine Offset Calibration
A static reference and a VDDA-dependent reference voltage are available for offset calibration. The static reference is suitable for external sensors that provide stable and self-regulated signals, and the VDDA-dependent reference fits various XMR sensor bridges. Before offset calibration, the reference source must first be selected via the REFVOS register.

REFVOS(1:0)	Bank 0x3, Addr. 0x00, bit 5:4	Reset: 0x0
Code	Function	
0x0	Static	
0x1	VDDA_3V	
0x2	reserved	
0x3	VDDA_5V	

Table 11: Offset Reference Source

The offset calibration is adjusted using the registers OFS and OFC and depends on the selected REFVOS source. A positive sensor offset is compensated with a positive value at OFS or OFC.

OFS(3:0)	Bank 0x3, Addr. 0x05, bit 7:4	Reset: 0x0
OFS(11:4)	Bank 0x3, Addr. 0x06, bit 7:0	Reset: 0x00
OFC(3:0)	Bank 0x3, Addr. 0x07, bit 7:4	Reset: 0x0
OFC(11:4)	Bank 0x3, Addr. 0x08, bit 7:0	Reset: 0x00
Code	Offset	
0x000	0.000 mV	
...	+1000 mV∗*Code*/2047	
0x7FF	1000.000 mV	
0x800	−1000.000 mV (equal to 0x801)	
0x801	−1000.000 mV	
...	−1000 mV∗(4096 − *Code*)/2047	
0xFFF	−0.489 mV	
Notes	Values calculated for REFVOS = 0.	

Table 12: Offset Correction Sine and Cosine

Sine to Cosine Phase Correction
If the signal phase between sine and cosine deviates from 90 degrees, correction is possible via the PH and PHMAX registers, whereas the latter parameter determines the maximum correction range.

PHMAX	Bank 0x3, Addr. 0x00, bit 6	Reset: 0
Code	Value	
0	11 °	
1	40 °	

Table 13: Phase Adjustment Range

PH(2:0)	Bank 0x3, Addr. 0x09, bit 7:5	Reset: 0x0
PH(10:3)	Bank 0x3, Addr. 0x0A, bit 7:0	Reset: 0x00
Code	Phase correction	
	PHMAX = 0	PHMAX = 1
0x000	0.000 °	0.000 °
0x001	0.006 °	0.020 °
...	11 °∗(*Code* − 1)/1022	40 °∗(*Code* − 1)/1022
0x3FF	11.000 °	40.000 °
0x400	equal to 0x401	
0x401	-11.000 °	-40.000 °
...	-11 °∗(2047 − *Code*)/1022	-40 °∗(2047 − *Code*)/1022
0x7FE	-0.011 °	-0.039 °
0x7FF	-0.006 °	-0.020 °

Table 14: Phase Correction

Test Modes for Signal Calibration

The operating mode of the iC-NQE can be altered for signal calibration and function tests.

Table 15 summarizes the test modes that are relevant for **analog signal adjustments** and for which the output function of A, B, SDA, SCL or PSO, NSO, PCO, NCO is changed (see also Figure 16).

Table 16 summarizes the test modes that are relevant for **digital signal adjustments** and for which the output function of A, B, and Z is changed.

TMA(7:0)	Bank 0x0, Addr. 0x02, bit 7:0	Reset: 0x00
TMA(15:8)	Bank 0x0, Addr. 0x03, bit 7:0	Reset: 0x00
Code	Function	
0x0000	Normal Operation	
0x0141	Analog Calibration Signals at A/B/SDA/SCL	
0x0181	Analog Calibration Signals at PSO/NSO/PCO/NCO	
0x0441	Sensor Signals at A/B/SDA/SCL	
0x0481	Sensor Signals at PSO/NSO/PCO/NCO	
Others	Not permitted	
Notes	Alias name TMA or TMA1 = 0x0141 Alias name TMA2 = 0x0181 Alias name TSA or TSA1 = 0x0441 Alias name TSA2 = 0x0481 Modes TMA2 and TSA2 require EN_ADRV = 1.	

Table 15: Analog Calibration Mode

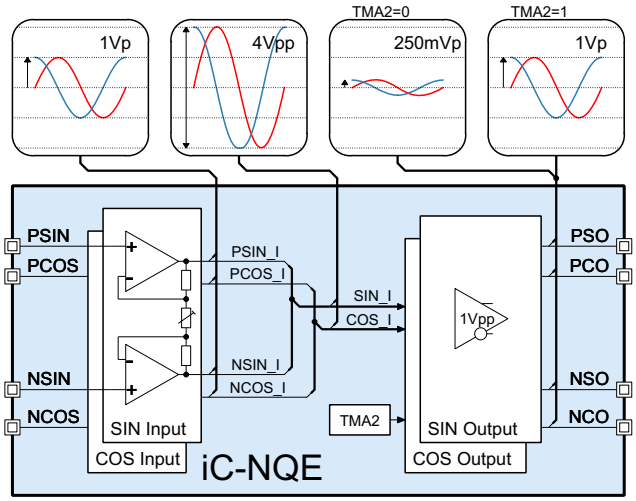

Figure 16: Analog Calibration Signal Output

Parameter CALIB_EN enables digital calibration modes which provide test signals at the A, B and Z outputs either for offset and phase, or offset and amplitude ratio.

In this case, the signal correction parameters OFS, OFC, and PH as well as GFS versus GFC must be adjusted to generate a pulse-to-pause ratio of 50 % for the corresponding test signal. The recommended trimming order (after selecting GAIN) is offset, phase, amplitude ratio and offset.

CALIB_EN(1:0)	Bank 0x0, Addr. 0x00, bit 1:0	Reset: 0x0
Code	Function	
0x0	Normal Operation	
0x1	Calibration signals for Offset and Phase at A/B/Z	
0x2	Calibration signals for Offset and Ratio at A/B/Z	
Others	Not permitted	

Table 16: Digital Calibration Mode

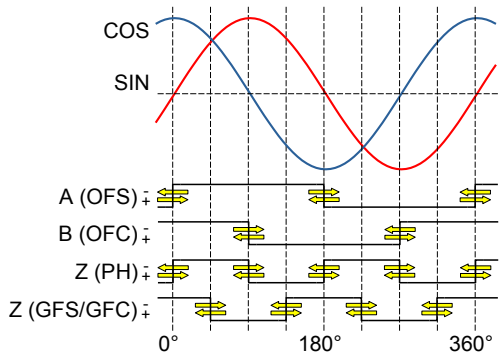

Figure 17: Digital Calibration Signal Output

Permissible Differential Input Voltages

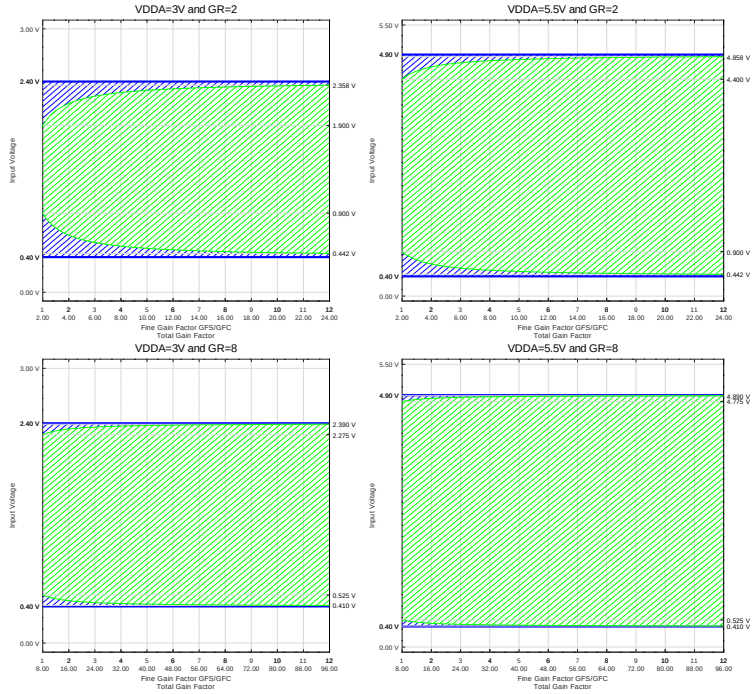

Figure 18: Permissible Input Voltage (blue) and Common Mode Voltage (green) Range for ISM = 0x0, 0x2, 0x3

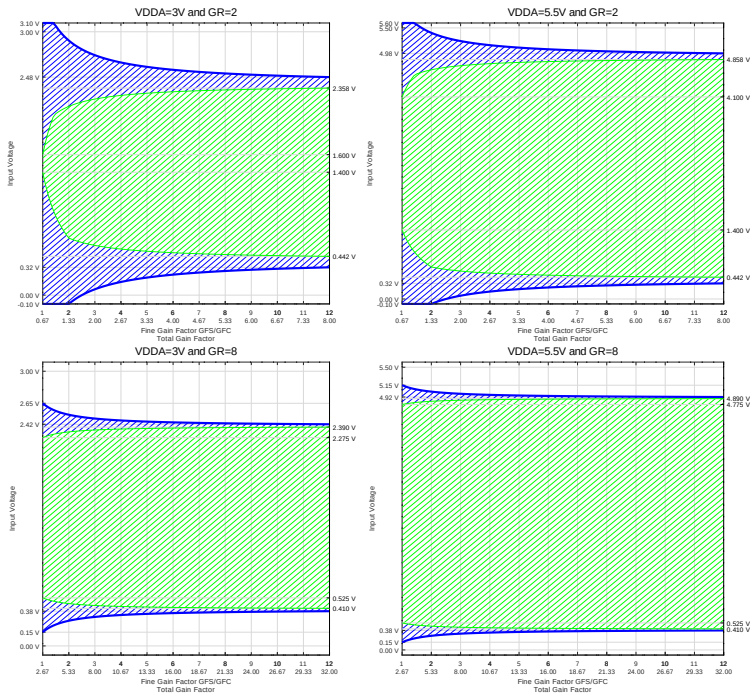

Figure 19: Permissible Input Voltage (blue) and Common Mode Voltage (green) Range for ISM = 0x4

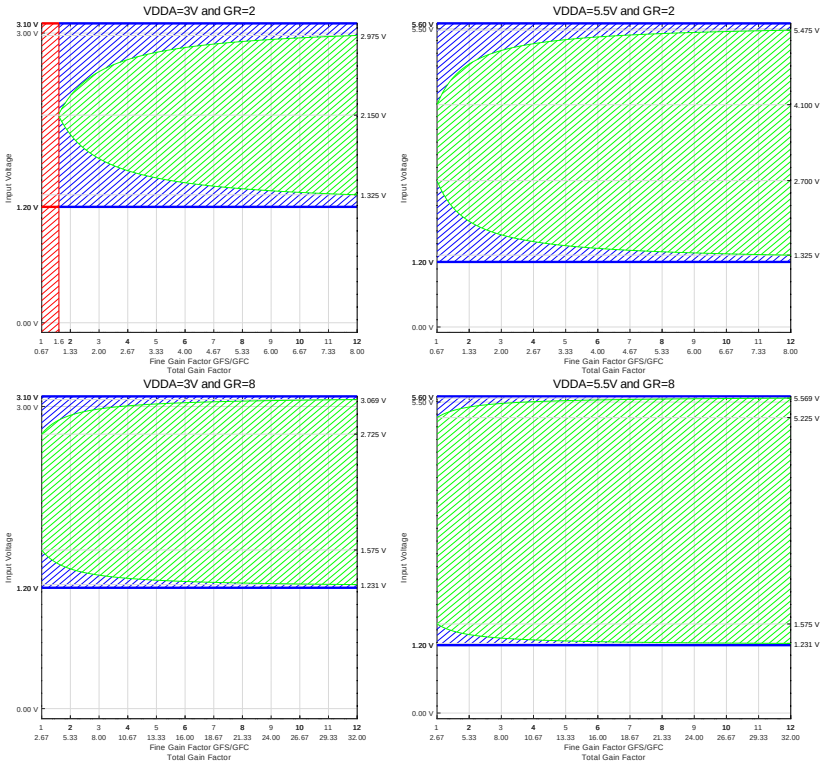

Figure 20: Permissible Input Voltage (blue) and Common Mode Voltage (green) Range for ISM = 0x5

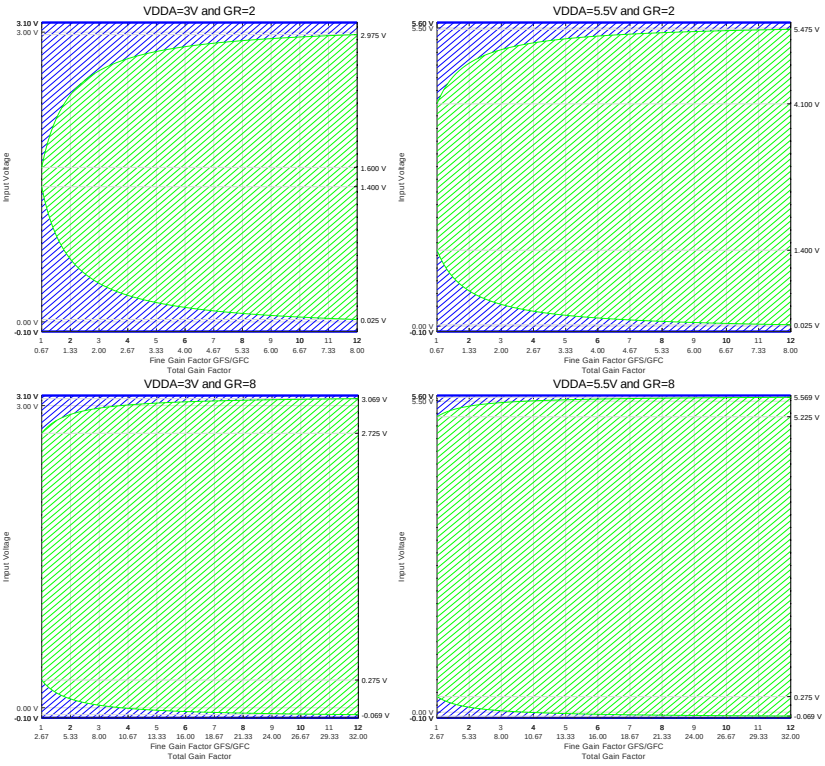

Figure 21: Permissible Input Voltage (blue) and Common Mode Voltage (green) Range for ISM = 0x7

SIGNAL MONITORING

The signal monitoring circuit of the iC-NQE provides a *square sum* and a *minimum* signal amplitude monitoring method.

Square Sum Signal Amplitude Monitoring

This monitoring circuit generates a constant voltage AMP with a linear relation to the chip's internal signal amplitudes (see Figures 1 and 16) according to the formula:

$$AMP = SIN\_I^2 + COS\_I^2$$

Figure 22 shows the circular XY-plot of AMP as obtained from the equation.

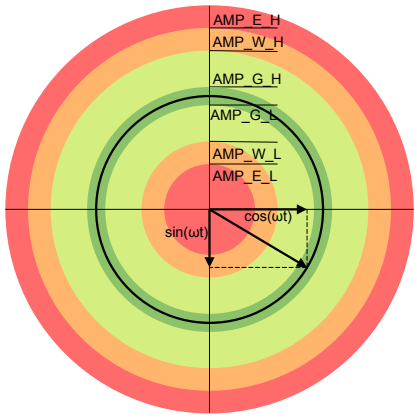

Figure 22: Square Sum Signal Amplitude Monitoring.

The amplitude signal AMP is compared with a group of threshold voltages generating flags for gain control, warning and error (see Tables 17 and 18).

AMP_G_L	Addr. 0x6A, bit 0	Read only
AMP_W_L	Addr. 0x6A, bit 2	Read only
AMP_E_L	Addr. 0x6A, bit 4	Read only
Code	Function	
0	Not OK, Gain needs to be increased	
1	OK, Amplitude is higher than minimum threshold	

Table 17: Square Sum Low Level Monitoring

AMP_G_H	Addr. 0x6A, bit 1	Read only
AMP_W_H	Addr. 0x6A, bit 3	Read only
AMP_E_H	Addr. 0x6A, bit 5	Read only
Code	Function	
0	OK, Amplitude is lower than maximum threshold	
1	Not OK, Gain needs to be decreased	

Table 18: Square Sum High Level Monitoring

The threshold voltages are configured by the parameters AMPT_EW, AMPT_G_L and AMPT_G_H. Additionally, parameter REFAMPL selects between a constant or a supply dependent reference VRA.

REFAMPL	Bank 0x3, Addr. 0x0B, bit 3	Reset: 0
Code	Function	
0	VRA = VREF (typ. VDDA / 2)	
1	VRA = 2 × VBG	
Notes	Refer to Elec. Char. No. 220 for VBG. Refer to Elec. Char. No. 321 for VREF. Use DIS_VREF = 1 for external VREF supply.	

Table 19: Square Sum Monitoring Reference

AMPT_EW(1:0)	Bank 0x3, Addr. 0x0B, bit 1:0	Reset: 0x0
Code	Warning[1]	Error[1]
	REFAMPL = 1	
0x0	1.4 Vpp ↔ 4.6 Vpp	1.0 Vpp ↔ 4.9 Vpp
0x1	2.0 Vpp ↔ 4.6 Vpp	1.4 Vpp ↔ 4.9 Vpp
0x2	2.6 Vpp ↔ 4.6 Vpp	2.0 Vpp ↔ 4.9 Vpp
0x3	2.9 Vpp ↔ 4.6 Vpp	2.6 Vpp ↔ 4.9 Vpp
	REFAMPL = 0	
0x0	? %VREF ↔ ? %VREF	? %VREF ↔ ? %VREF
0x1	? %VREF ↔ ? %VREF	? %VREF ↔ ? %VREF
0x2	? %VREF ↔ ? %VREF	? %VREF ↔ ? %VREF
0x3	? %VREF ↔ ? %VREF	? %VREF ↔ ? %VREF
Notes	Refer to Figure 16 for the explanation of amplitude. [1] All values are typical referred to SIN_I and COS_I; see Elec. Char. No. 701 and 702 for tolerances.	

Table 20: Square Sum Monitoring Thresholds for Warning and Error

AMPT_G_H(2:0)	Bank 0x3, Addr. 0x0C, bit 2:0	Reset: 0x0
AMPT_G_L(2:0)	Bank 0x3, Addr. 0x0C, bit 5:3	Reset: 0x0
Code	Gain Low[1]	Gain High[1]
0x0	2.9 Vp	3.1 Vp
0x1	3.1 Vp	3.3 Vp
0x2	3.3 Vp	3.5 Vp
0x3	3.5 Vp	3.7 Vp
0x4	3.7 Vp	3.9 Vp
0x5	3.9 Vp	4.1 Vp
0x6	4.1 Vp	4.3 Vp
0x7	4.3 Vp	4.5 Vp
Notes	Refer to Figure 16 for the explanation of amplitude. [1] All values are typical referred to SIN_I and COS_I; see Elec. Char. No. 705 and 706 for tolerances. Use REFAMPL = 1 for gain control.	

Table 21: Square Sum Amplitude Thresholds for Gain Control

Minimum Signal Level Monitoring

This monitoring circuit determines the maximum value of the internal signals SIN_I, NSIN_I, COS_I and NCOS_I and compares it with the threshold voltage Vth()min. If the threshold is undershot, the amplitude error flag AMP_E_M is set.

A selection of threshold voltages, which all depend on VDDA, is possible using AMP_EW

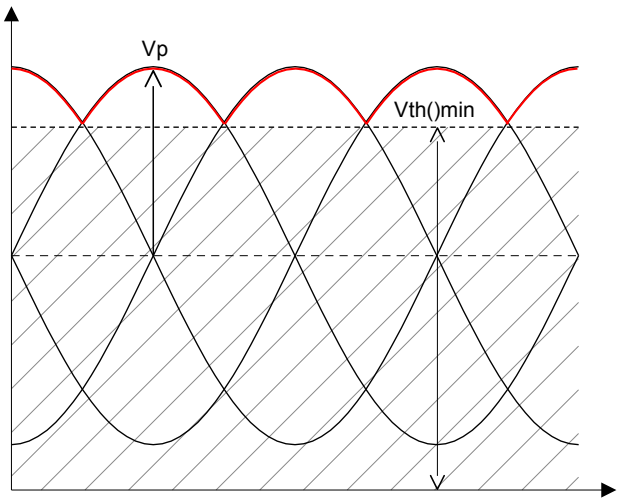

Figure 23: Minimum Level Monitoring

AMP_E_M	Addr. 0x6A, bit 6	Read only
Code	Function	
0	Not OK, Amplitude resp. Gain needs to be increased	
1	OK, Amplitude is higher than minimum threshold	

Table 22: Minimum Monitoring Error Comparator

AMPT_EW(1:0)	Bank 0x3, Addr. 0x0B, bit 1:0		Reset: 0x0
Code	Vth()min[1]	Internal Signal Amplitude[2] VDDA = 3.3 V	Internal Signal Amplitude[2] VDDA = 5 V
0x0	0.57 × VDDA	0.327 Vp	0.495 Vp
0x1	0.59 × VDDA	0.420 Vp	0.636 Vp
0x2	0.60 × VDDA	0.490 Vp	0.742 Vp
0x3	0.62 × VDDA	0.560 Vp	0.849 Vp
Notes	Refer to figure 23 for the explanation of amplitude. [1] All values are typical; see Elec. Char. No. 707 for tolerances. [2] All values are typical referred to SIN_I and COS_I; VREF = VDDA/2		

Table 23: Minimum Level Monitoring Threshold

AUTOMATIC GAIN CONTROL

The gain control circuit is enabled with GC_EN and evaluates the high level monitoring flag AMP_G_H, and if selected by GC_2C, the low level monitoring flag AMP_G_L in addition.

The corresponding level monitoring thresholds AMPT_G_H and AMPT_G_L define the control's set-points and must be suitably configured in advance (see chapter SIGNAL MONITORING, page 36).

When GC_2C selects to operate on both flags, a gain step as per GC_2CVAL is executed as soon as the signal amplitude leaves the monitoring window defined by the high and low level comparators.

GC_EN	Bank 0x3, Addr. 0x0B, bit 4	Reset: 0
Code	Function	
0	Gain control disabled	
1	Gain control enabled	

Table 24: Gain Control Enable

GC_2C	Bank 0x3, Addr. 0x0B, bit 6	Reset: 0
Code	Function	
0	Gain control with comparator AMP_G_H	
1	Gain control with comparators AMP_G_L and AMP_G_H	

Table 25: Gain Control Window

GC_2CVAL	Bank 0x3, Addr. 0x0B, bit 7	Reset: 0
Code	Value	
0	1	
1	41	

Table 26: Gain Step

Regular control operation adjusts only the fine gains GFS and GFC. However, the control operation can be enabled by GC_I_GR to also adapt the coarse gain GR if required.

GC_I_GR	Bank 0x3, Addr. 0x0B, bit 5	Reset: 0
Code	Function	
0	Control of fine gain	
1	Control of coarse and fine gain	

Table 27: Coarse Gain Control

Note: The analog calibration registers GR, GFS, OFS, OFC, PH must not be changed while automatic gain control is active.

Gain adaptions are carried out on internal shadow registers, namely GC_GFS an GC_GR which could be read back for inspection. Since actually no configuration parameter is overwritten, the checksum for the configuration remains unchanged and the CRC_CALC command can still be used.

GC_GFS(7:0)	Addr. 0x66, bit 7:0	Read only
GC_GFS(11:8)	Addr. 0x67, bit 3:0	Read only
Code	Value	
0x000	1.0	
...	$12.0^{(Code/4095)}$	
0xFFF	12.0	

Table 28: Gain Control Fine Factor

GC_GR	Addr. 0x67, bit 4	Read only
Code	Value	
0	2	
1	8	

Table 29: Gain Control Coarse Factor

If the gain control reaches its limits and the gain cannot be increased or decreased further, this is reported in the flags GC_ERR_H and GC_ERR_L.

SINE-TO-DIGITAL CONVERTER

The iC-NQE digitizes the sin/cos input signals with a vector-tracking converter according to Figure 24, where the phase shift of the signal controls a counter representing the interpolated angle POS_IA to move up or down.

The circuit operates according to the theorem of angle addition:

$$sin(\alpha + \beta) = sin(\alpha) * cos(\beta) + cos(\alpha) * sin(\beta)$$

The transfer functions for COS and SIN are predefined, but adjustable to a certain degree (see section Integrated Linearization).

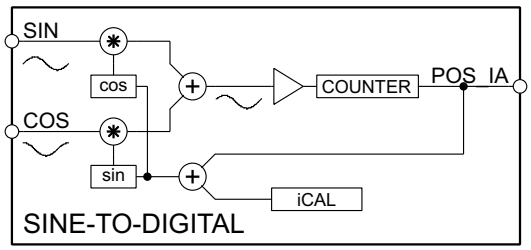

Figure 24: Sine-to-Digital Converter Principle

The value of POS_IA increases when the COS signal leads the SIN signal at the inputs. The zero position can be set in steps of 90 degrees with ZERO_POS, which may be necessary if masking of the Z output with the ZERO input is activated by ABZ_ZMSK.

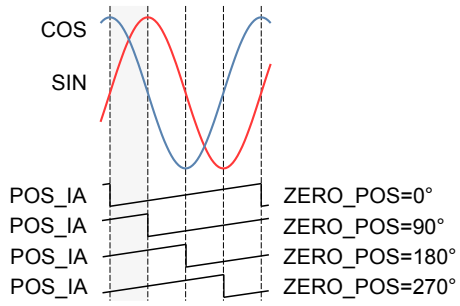

Figure 25: Sine-to-Digital Converter Zero Position

ZERO_POS(1:0)	Bank 0x4, Addr. 0x01, bit 5:4	Reset: 0x0
Code	Function	
0x0	0 Deg	
0x1	90 Deg	
0x2	180 Deg	
0x3	270 Deg	

Table 30: Zero Position

Hysteresis

The digital angular hysteresis separates the switching points of the converter between CW and CCW operation. It thus eliminates spurious switching at standstill if the hysteresis configuration HYS_CFG is set sufficiently high relative to the input noise.

HYS_CFG(3:0)	Bank 0x4, Addr. 0x01, bit 3:0	Reset: 0x0
Code	Value	
0x0	0.0 °	
0x1	0.0220 °	
0x2	0.0439 °	
0x3	0.0879 °	
0x4	0.1758 °	
0x5	0.3516 °	
0x6	0.7031 °	
0x7	1.4062 °	
0x8	2.8125 °	
0x9	5.6250 °	
Others	Not permitted	

Table 31: Hysteresis Configuration

The hysteresis configuration only affects the ABZ GENERATOR by default, but can also be enabled for all serial interfaces with HYS_EN.

HYS_EN	Bank 0x4, Addr. 0x04, bit 0	Reset: 0
Code	Function	
0	Hysteresis only used for ABZ GENERATOR	
1	Hysteresis used for all interfaces	

Table 32: Hysteresis Enable (serial interfaces)

Digital Position Filter

With FILT_EN a digital loop filter can be activated to obtain smoother interpolation data. The parameters of the filter are preset internally, for which CFGFILT provides a selection of user settings.

FILT_EN	Bank 0x4, Addr. 0x03, bit 0	Reset: 0
Code	Function	
0	Disabled (classic conversion)	
1	Enabled (filtered conversion)	

Table 33: Filter Enable

CFGFILT(2:0)	Bank 0x4, Addr. 0x03, bit 6:4	Reset: 0x0
Code	Value	
0x0	0 (fast)	
0x1	1	
0x2	2	
0x3	3	
0x4	4	
0x5	5	
0x6	6	
0x7	7 (slow)	

Table 34: Filter Presets

Integrated Linearization

iC-NQE can compensate for an input signal distortion to a certain degree by adjusting the converter's transfer function. The adaption is enabled with ICAL_EN and employs 1024 byte of RAM providing Linearization Data. The Linearization Data (iCAL) is accessible via the banks 16 to 31.

Every single byte of the correction data affects the transfer function at a corresponding angular position. Thereby the iCAL Correction Factor ICAL_FAC selects the weighting for all bytes together. For example, if a resolution of 79 ” is set, the maximum correction is ±2.8° at each node.

ICAL_EN	Bank 0x4, Addr. 0x03, bit 1	Reset: 0
Code	Function	
0	iCAL Correction disabled	
1	iCAL Correction enabled	

Table 35: iCAL Correction Enable

iCAL(1023:0)	Bank 0x10 .. Bank 0x1F
Code	Function
Signed (2k)	Linearization Data

Table 36: Linearization Data

ICAL_FAC(1:0)	Bank 0x4, Addr. 0x03, bit 3:2	Reset: 0x0
Code	Value	Max. Correction Range PCR_ML = 1 (256) cpr
0x0	79 ”	±2.8° (±39”)
0x1	158 ”	±5.6° (±78”)
0x2	316 ”	±11.1° (±157”)
0x3	633 ”	±22.3° (±314”)

Table 37: iCAL Correction Factor

Classic Conversion

The classic conversion mode is implemented for backwards compatibility with iC-NQC and is automatically enabled whenever the digital position filtering is turned off (by FILT_EN = 0). In this case, the converter frequency automatically adjusts to the value required to track the input frequency at the resolution programmed with SELRES.

SELRES(3:0)	Bank 0x4, Addr. 0x00, bit 3:0	Reset: 0x0
Code	Value	
0x0	Not permitted	
0x1	Not permitted	
0x2	16384	
0x3	8192	
0x4	4096	
0x5	2048	
0x6	1024	
0x7	512	
0x8	256	
0x9	128	
0xA	64	
0xB	32	
0xC	16	
0xD	8	
0xE	4	
0xF	2	

Table 38: Resolution (classic conversion)

With SUBDIV, automatic reduction of the converter resolution can be allowed so that the converter can follow an even higher input frequency. If the input signals then exceed the frequency limit of the configured resolution, the converter continues tracking at half the resolution and synthesizes the LSB. When the next frequency limit is exceeded, the LSB and LSB +1 are synthesized, and so on. When the input signals slow down and the frequency drops below the threshold values again, fine resolution automatically returns.

SUBDIV(1:0)	Bank 0x4, Addr. 0x00, bit 5:4	Reset: 0x0
Code	Max. Input Frequency	Restriction
0x0	fosc()min / 8 / Resolution	
0x1	fosc()min / 4 / Resolution	Rel. angle error x2
0x2	fosc()min / 2 / Resolution	Rel. angle error x4
0x3	fosc()min / 1 / Resolution	Rel. angle error x8

Table 39: Adaptive Increments (classic conversion)

In the classic conversion mode, the incremental output signals A, B and Z can be derived directly from the converter according to the selected resolution without using the FlexCount® generator (see chapter ABZ GENERATOR on page 46).

FLEX_DIS	Bank 0x4, Addr. 0x00, bit 6	Reset: 0
Code	Function	
0	FlexCount® enabled	
1	FlexCount® disabled	

Table 40: FlexCount® Disable

ZERO INPUTS and PERIOD COUNTER

Zero Input Comparator

The comparator which evaluates the PZERO and NZERO inputs can be enabled to reset the period counter. For this purpose a configuration is possible, where only the very first or each index signal clears the counter.

PCR_CPZ enables clearing the counter for each index, while PCR_CPZ1 allows the same only for the very first index. If both options are deactivated, the period counter is cleared when iC-NQE is reset, e.g. by the NRES pin or when cycling power. Furthermore, counter changes can be controlled by the ADI (if in use) or via preset commands.

PCR_CBZ	Bank 0x5, Addr. 0x00, bit 6	Reset: 0
Code	Function	
0	Disabled	
1	Clear period counter by every zero	

Table 41: Period Counter Clear by Zero

PCR_CBZ1	Bank 0x5, Addr. 0x00, bit 7	Reset: 0
Code	Function	
0	Disabled	
1	Clear period counter by first zero	

Table 42: Period Counter Clear by First Zero

If the PZERO/NZERO inputs are not required to process an index signal, the comparator can be switched off with EN_ZERO to save power.

EN_ZERO	Bank 0x2, Addr. 0x01, bit 5	Reset: 0
Code	Function	
0	Zero comparator disabled	
1	Zero comparator enabled	

Table 43: Zero Input Comparator Enable

Period Counter

The internal period counter tracks the overflow and underflow of the sine-to-digital converter. In addition, a fast two-bit interpolator with comparators at the sin/cos inputs can be enabled via PCR_FC to speed up the period counting. When used, a counter error is displayed on ERR_IA_C if the interpolated angle lags by more than 45 degrees.

PCR_FC	Bank 0x5, Addr. 0x01, bit 4	Reset: 0
Code	Function	
0	Forced period counting disabled	
1	Forced period counting enabled	

Table 44: Forced Period Counting

Mechanical and Total Counter Length

Since encoder devices may read more than one sin/cos cycle per revolution, the iC-NQE can be configured for the number of input cycles per revolution. This allows the singleturn position to be generated over 360 mechanical degrees.

The parameter PCR_TL defines the total bit count used for the period counting, and additionally the parameter PCR_ML defines the number of input cycles per mechanical revolution.

PCR_TL(5:0)	Bank 0x5, Addr. 0x00, bit 5:0	Reset: 0x00
Code	Bit length	
0x00	0	
...	*Code*	
0x20	32	
Others	Not permitted	

Table 45: Period Counter Total Length

PCR_ML(3:0)	Bank 0x5, Addr. 0x01, bit 3:0	Reset: 0x0
Code	Input cyles per revolution	
0x0	1	
...	2^{Code}	
0x8	256	
Others	Not permitted	
Notes	PCR_ML must not exceed PCR_TL.	

Table 46: Period Counter Mech. Length

ABSOLUTE DATA INTERFACE (ADI)

The Absolute Data Interface (ADI) is a configurable synchronous serial interface that occupies the PZERO and NZERO pins. The clock signal ACL is output to PZERO, the ADA data is taken back via NZERO.

The interface features an SSI master that cyclically reads position data from the external sensor (the slave), which is used to initialize and monitor the chip's internal period counter. Table 47 summarizes the ADI performance at a glance.

ADI Key Parameters		
Protocol	SSI	BiSS
Header	None	Standard, w. start bit delay, CDS ignored
Coding	Binary or Gray	Binary
CRC	n/a	6 bit, polyn. 0x43, start value 0
Clock frequency	150 kHz or 1.5 MHz	
Frame repetition	1.5 ms (normal operation) 0.2 ms (fast startup)	
Slave timeout	10 µs. . . 40 µs	
PCR data length	1 . . . 32 bit	

Table 47: ADI Performance

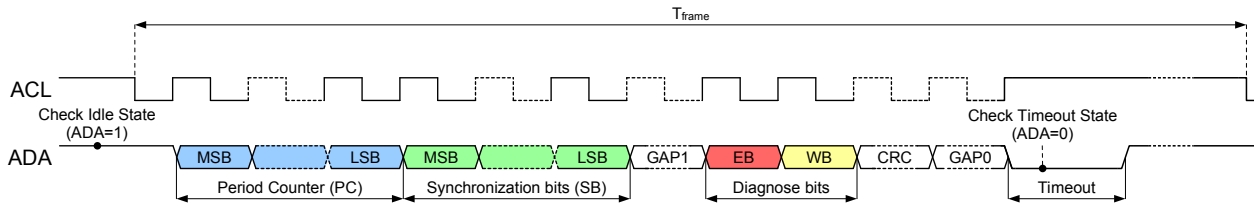

Figure 26: ADI Communication (with SSI)

ADI Enable and Synchronization

If the ADI master is enabled with ADI_EN, the received position data consisting of period counter bits (PCR_TL) and additional synchronizations bits are synchronized to the interpolated angle.

ADI_EN	Bank 0x5, Addr. 0x03, bit 0	Reset: 0
Code	Function	
0	ADI disabled	
1	ADI enabled	

Table 48: ADI Enable

The synchronized data is then compared with the internal period counter that was initialized during startup. In case of a position mismatch the error ADI_PCR is generated and, depending on the parameters ADI_PRIO and ADI_DERR, the period counter can be updated.

ADI_PRIO	Bank 0x5, Addr. 0x03, bit 6	Reset: 0
Code	Function	
0	Keep internal PCR	
1	Always use external PCR	

Table 49: External PCR Data Priority (ADI)

ADI_DERR	Bank 0x5, Addr. 0x03, bit 7	Reset: 0
Code	Function	
0	Report errors immediately	
1	Mask single errors (keep internal PCR)	

Table 50: Double Error Messaging (ADI)

The number of available synchronization bits determines the width of the synchronization range and thus the tolerable phase shift. A maximum of 4 synchronization bits is possible and can be set via ADI_SBL.

ADI_SBL(2:0)	Bank 0x5, Addr. 0x02, bit 2:0	Reset: 0x0
Code	Synchronization bits	Phase Shift Range
0x0	0	no synchronization
0x1	1	± 90 °
0x2	2	± 135 °
0x3	3	± 157.5 °
0x4	4	± 168.75 °
Others	Not permitted	

Table 51: Synchronization Bit Length (ADI)

The optimum phase shift of the incoming data would be in the middle of the synchronization range (0° aligned). However, a non-ideal mounting of the sensor on the ADI compared to the sin/cos sensor can be compensated by adjusting the synchronization offset ADI_OFS accordingly.

ADI_OFS(4:0)	Bank 0x5, Addr. 0x02, bit 7:3	Reset: 0x00
Code	Value	
0x00	0.00 °	
...	11.25 °∗*Code*	
0x1F	348.75 °	

Table 52: Synchronization Offset (ADI)

Synchronization Warning Limit
To monitor the data synchronization, a warning threshold can be set up with ADI_SWL. When this threshold is reached, WRN_ADI is activated.

ADI_SWL(1:0)	Bank 0x5, Addr. 0x04, bit 5:4	Reset: 0x0
Code	Function	
0x0	Disabled	
0x1	+/-45 °	
0x2	+/-90 °	
0x3	+/-135 °	

Table 53: Synchronization Warning (ADI)

Raw Data Access
This special mode allows to access the unsychronized position data of each ADI communication in single-slave operation.

ADI_RAW	Bank 0x5, Addr. 0x04, bit 7	Reset: 0
Code	Function	
0	Raw data mode disabled	
1	Raw data mode enabled	

Table 54: Raw Data Mode (ADI)

When raw data mode is activated, the period counter is not updated based on the interpolated angle POS_IA, but with the unsynchronized data from each ADI communication. In addition, the output of the interpolation data changes: the interpolation value is now only updated for each ADI communication and supplemented by the synchronization bits that were received with the last ADI communication.

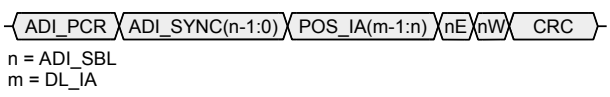

Figure 27: BiSS Output Format in Raw Data Mode.

Daisy-chaining both sensors, the ADI (multiturn) sensor with the sin/cos (singleturn) sensor can be considered using ADI_GET, allowing an inspection of the phase relation.

ADI_GET	Bank 0x5, Addr. 0x04, bit 1	Reset: 0
Code	Function	
0	Chain mode disabled	
1	Chain mode enabled	

Table 55: ADI Chain Mode (for BiSS only)

Error and Warning Bits
If the ADI sensor provides the position data with error and warning bits, the ADI can be configured to process this diagnostic information. Their availability is set with ADI_EBL and ADI_WBL, and the polarity is configured with ADI_DBP.

ADI_EBL	Bank 0x5, Addr. 0x03, bit 2	Reset: 0
Code	Function	
0	No error bit in ADI data stream	
1	One error bit in ADI data stream	

Table 56: ADI Error Bit Length

ADI_WBL	Bank 0x5, Addr. 0x03, bit 3	Reset: 0
Code	Function	
0	No warning bit in ADI data stream	
1	One warning bit in ADI data stream	

Table 57: ADI Warning Bit Length

ADI_DBP	Bank 0x5, Addr. 0x03, bit 4	Reset: 0
Code	Function	
0	Active low	
1	Active high	

Table 58: ADI Diagnostic Bit Polarity

Gap Bits
If the external sensor provides more bits than are required for processing its position data, gap bits can be configured for mapping.
ADI_GAP1 defines the number of bits to be dumped between the synchronization and the diagnostic bits, and ADI_GAP0 the number of bits to be dumped at the end of the frame (e.g. additional diagnostic or checksum bits). The latter must be defined because the ADA pin status is checked (the frame must end with zero).

ADI_GAP1(4:0)	Bank 0x5, Addr. 0x06, bit 4:0	Reset: 0x00
Code	Value	
0x00	0	
...	*Code*	
0x1F	31	

Table 59: Trailing Sync Gap Bits (ADI)

ADI_GAP0(4:0)	Bank 0x5, Addr. 0x05, bit 4:0	Reset: 0x00
Code	Value	
0x00	0	
...	*Code*	
0x1F	31	

Table 60: Trailing Gap Bits (ADI)

Clock Frequency and Coding
The ADI clock frequency is selectable with ADI_CF and must match the allowed clock frequency of the sensor. The ADI input format is configurable with ADI_GRAY.

ADI_CF	Bank 0x5, Addr. 0x03, bit 1	Reset: 0
Code	Value	
0	150 kHz	
1	1500 kHz	

Table 61: ADI Clock Frequency

ADI_GRAY	Bank 0x5, Addr. 0x03, bit 5	Reset: 0
Code	Function	
0	Position data in binary code	
1	Position data in gray code	
Notes	The input format refers to the position data only and not the diagnostic bits.	

Table 62: ADI Input Format (for PCR+SB)

BiSS Mode
The ADI can process data from BiSS slaves and supports the start sequence of the BiSS protocol, including an optional delay of the start bit.

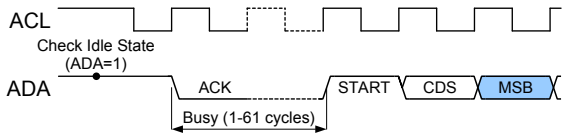

Figure 28: ADI Communication With BiSS Start Sequence.

ADI_BISS	Bank 0x5, Addr. 0x04, bit 2	Reset: 0
Code	Function	
0	SSI mode used	
1	BiSS mode used	

Table 63: BiSS Mode Enable (ADI)

The ADI slave can request additional processing time by delaying the start bit by up to 60 additional ACL clock cycles. iC-NQE monitors the BiSS start sequence but ignores the CDS bit. If a violation occurs or no start bit is detected, ERR_ADI becomes active and ADI_FRM is set to 0x1.

If the CRC evaluation is activated by ADI_CRC, the 6-bit BiSS standard CRC with polynomial 0x43 and start value 0 is verified. As usual, the CRC bits must be inverted by the slave before transmission. A CRC error is reported by an active ERR_ADI and the value 0x2 at ADI_FRM.

ADI_CRC	Bank 0x5, Addr. 0x04, bit 3	Reset: 0
Code	Function	
0	No CRC evaluation*	
1	6-bit CRC evaluation (polynomial 0x43, start value 0)	
Note	*) Configure gap bits for replacement.	

Table 64: BiSS CRC Evaluation (ADI)

ADI Startup
During system startup, also Reset command, the ADI master cyclically tries to read data from the ADI slave. If the slave is not yet ready (signaled by ADA = const = 1 or ADA = const = 0, which is recommended), the ADI master remains in the startup phase (indefinitely).

Once a valid communication with the ADI slave is established, the startup phase is not terminated immediately. To exit the startup phase successfully, two consecutive communication cycles must be valid (without protocol errors), the period counter must be OK when checked with the external data, and no error bit must be set in the protocol.

If all these conditions are met, the interface continues with normal operation. The cycle time at startup can be shortened with ADI_FSTP if needed.

ADI_FSTP	Bank 0x5, Addr. 0x04, bit 0	Reset: 0
Code	Function	
0	Normal cycle time during startup	
1	Short cycle time during startup	

Table 65: ADI Fast Startup

Dual Input Mode
If iC-NQE evaluates a sensor that provides two sinusoidal signal periods per mechanical revolution, an AMR angle sensor for instance, using the Dual Input Mode could be considered to differentiate between the first and second half of the mechanical revolution. In this mode, the PZERO and NZERO inputs are altered to evaluate a sector information, i.e. a 2-bit Gray code provided by a multiturn position sensor.

ADI_DUAL	Bank 0x5, Addr. 0x04, bit 6	Reset: 0
Code	Function	
0	Dual input mode disabled	
1	Dual input mode enabled	

Table 66: Dual Input Mode Enable (ADI)

ABZ GENERATOR

The ABZ generator uses the FlexCount® function to convert the absolute angular position into incremental (quadrature) signals. This generator function and the output on the A, B and Z pins is enabled by EN_ABZ.

EN_ABZ	Bank 0x2, Addr. 0x01, bit 2	Reset: 0
Code	Function	
0	ABZ output disabled	
1	ABZ output enabled	

Table 67: ABZ Output Enable

Note: For ABZ output in classic conversion mode, the FlexCount® function can be deactivated separately with FLEX_DIS.

AB Output Cycles

The number of AB cycles per mechanical revolution is configured with ABZ_CPR, where a mechanical revolution may contain one or more input periods as defined by the setting of PCR_ML.

ABZ_CPR(7:0)	Bank 0x6, Addr. 0x00, bit 7:0	Reset: 0x00
ABZ_CPR(15:8)	Bank 0x6, Addr. 0x01, bit 7:0	Reset: 0x00
ABZ_CPR(21:16)	Bank 0x6, Addr. 0x02, bit 5:0	Reset: 0x00
Code	Value	
0x000000	2^{22}	
0x000001	1	
...	*Code*	
0x3FFFFF	$2^{22} - 1$	

Table 68: AB Output Cycles

ABZ_CPR		
Code	AB Cycles Per Rev.	Edge Resolution
0x0001	1	4
0x03E8	1000	4000
0x0400	1024	4096
0x0FA0	4000	16000
0x1000	4096	16384
0x2710	10000	40000
0x4000	16384	65536

Table 69: Programming Examples of ABZ_CPR

AB Rotation Direction

The AB sequence provides information about the direction of rotation. If the interpolated angle POS_IA counts upwards because the cosine input leads the sine input, the quadrature signal is normally displayed with A before B. A reversal of the output direction is possible via ABZ_DIR. Figure 29 shows the correlation.

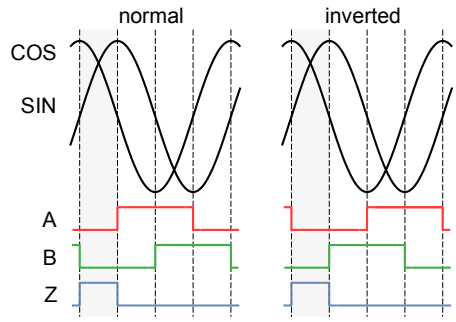

Figure 29: AB Rotation Direction

ABZ_DIR	Bank 0x6, Addr. 0x03, bit 0	Reset: 0
Code	Function	
0	Code direction normal	
1	Code direction reversed	

Table 70: AB Rotation Direction

Z Output Polarity and AB Phasing

The Z output can be AND-gated with the zero comparator result (i.e. with PZERO - NZERO) to output an index signal only once per mechanical revolution. For this function the zero comparator must be enabled by EN_ZERO and the masking selected by ABZ_ZMSK.

ABZ_ZMSK	Bank 0x6, Addr. 0x03, bit 3	Reset: 0
Code	Function	
0	Z unmasked	
1	Z masked with ZERO	

Table 71: Z Output Masking

The Z output polarity, if the index is high or low active, is selectable with ABZ_ZPOL.

ABZ_ZPOL	Bank 0x6, Addr. 0x03, bit 1	Reset: 0
Code	Function	
0	High active	
1	Low active	

Table 72: Z Output Polarity

The phase of A and B at the index position and the length of the Z pulse can be configured with ABZ_ABPH and ABZ_ZLEN. Figure 29 shows the options.

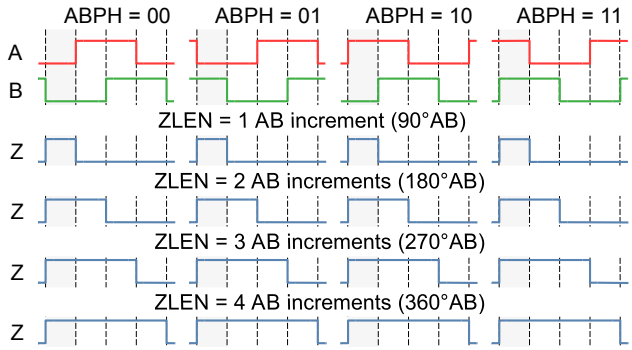

Figure 30: AB Phase and Z Length

ABZ_ZLEN(1:0)	Bank 0x6, Addr. 0x03, bit 7:6	Reset: 0x0
Code	Value	
0x0	1 AB increment	
0x1	2 AB increments	
0x2	3 AB increments	
0x3	4 AB increments	

Table 73: Z Output Length

ABZ_ABPH(1:0)	Bank 0x6, Addr. 0x03, bit 5:4	Reset: 0x0
Code	Function	
0x0	AB = 00	
0x1	AB = 01	
0x2	AB = 10	
0x3	AB = 11	

Table 74: AB Phasing

Hysteresis

As shown in Figure 31, the hysteresis set with HYS_CFG prevents unwanted switching of the ABZ outputs at the reversal point, e.g. when input direction changes from positive to negative. This is especially helpful at standstill to avoid output flicker due to sensor noise or interference at the inputs.

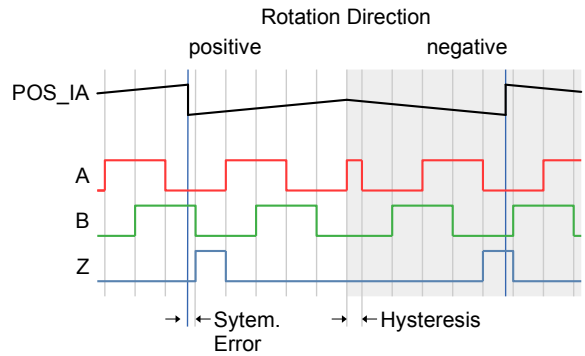

Figure 31: AB Hysteresis

The angular hysteresis results in a position slip between the two directions of rotation, causing a systematic angular error of half the hysteresis value.

HYS_CFG(3:0)	Bank 0x4, Addr. 0x01, bit 3:0	Reset: 0x0
Code	Function	
0x0	0 Deg	
0x1	0.0220 Deg	
0x2	0.0439 Deg	
0x3	0.0879 Deg	
0x4	0.1758 Deg	
0x5	0.3517 Deg	
0x6	0.7031 Deg	
0x7	1.4063 Deg	
0x8	2.8125 Deg	
0x9	5.625 Deg	

Table 75: Hysteresis Configuration

Minimum Transition Distance and Lag Detection

The minimum transition distance (MTD) limits the minimum time from edge to edge for the output signals A and B. If ABZ_MTD is configured according to the allowed maximum input frequency of the external counter or motor controller, fast sensor disturbances can be equalized and counting errors avoided.

ABZ_MTD(3:0)	Bank 0x6, Addr. 0x04, bit 3:0	Reset: 0x0
Code	tminTD() [1]	fmaxAB() [2]
0x0	12.5 ns	20 MHz
0x1	25.0 ns	10 MHz
0x2	37.5 ns	6.67 MHz
0x3	50.0 ns	5 MHz
0x4	75 ns	3.33 MHz
0x5	100 ns	2.5 MHz
0x6	125 ns	2 MHz
0x7	250 ns	1 MHz
0x8	500 ns	500 KHz
0x9	750 ns	333 KHz
0xA	1 µs	250 KHz
0xB	1.25 µs	200 KHz
0xC	2.5 µs	100 KHz
0xD	5 µs	50 KHz
0xE	7.5 µs	33.3 KHz
0xF	10 µs	25 KHz
Notes	[1] Calculated with $fosc_{min}$ = 80 MHz [2] Calculated with $fosc_{max}$ = 80 MHz (Refer to Electrical Characteristics, Item No. 101 on page 10)	

Table 76: Minimum Transition Distance

For example, if input changes would cause ABZ transitions that undershoot the allowed MTD (see column tminTD()), the output frequency is limited accordingly (see column fmaxAB()). In this case, the ABZ output will temporarily lag behind the input angle.

If this situation persists, an excessive output lag may occur where the vector-tracking conversion threatens to fail and could generate invalid ABZ signals (lag > 180°). Therefore, the iC-NQE monitors the output lag to trigger an alarm at an early stage before a fail-safe counting can no longer be guaranteed. ABZ_LAG defines the lag-threshold for generating an error message on ERR_ABZ.

ABZ_LAG(1:0)	Bank 0x6, Addr. 0x04, bit 5:4	Reset: 0x0
Code	Function	
0x0	ERR_ABZ not set	
0x1	ERR_ABZ set at lag $\geq \approx 22.5°$	
0x2	ERR_ABZ set at lag $\geq \approx 45°$	
0x3	ERR_ABZ set at lag $\geq \approx 90°$	

Table 77: Output Lag Monitoring

ABZ Position Offset

With ABZ_OFFS it is possible to shift the ABZ signals by an individual position offset against the internal angle.

ABZ_OFFS(7:0)	Bank 0x6, Addr. 0x05, bit 7:0	Reset: 0x00
ABZ_OFFS(15:8)	Bank 0x6, Addr. 0x06, bit 7:0	Reset: 0x00
ABZ_OFFS(23:16)	Bank 0x6, Addr. 0x07, bit 7:0	Reset: 0x00
Code	Value	
0x000000	0	
...	*Code*	
0xFFFFFF	$2^{24} - 1$	

Table 78: AB Output Phase Shift

Startup Control

ABZ_STUP configures the behavior of the ABZ outputs during startup.

ABZ_STUP	Bank 0x6, Addr. 0x03, bit 2	Reset: 0
Code	Function	
0	ABZ outputs idle during startup	
1	ABZ outputs active during startup	

Table 79: ABZ Startup Mode

UVW GENERATOR

The UVW generator, to be enabled with EN_UVW, can provide block commutation signals for motors with up to 32 pole pairs.

EN_UVW	Bank 0x2, Addr. 0x01, bit 3	Reset: 0
Code	Function	
0	UVW generator disabled	
1	UVW generator enabled	

Table 80: UVW Output Enable

UVW Output Cycles, Direction and Polarity

The number of UVW cycles per mechanical revolution is configured with UVW_CPR, where a mechanical revolution may contain one or more input periods as defined by the setting of PCR_ML.

UVW_CPR(4:0)	Bank 0x7, Addr. 0x00, bit 4:0	Reset: 0x00
Code	Function (number of pole pairs)	
0x00	32	
0x01	1	
...	*Code*	
0x1F	31	

Table 81: UVW Pole Pairs

The phase of U, V and W at the index position as well as the output sequence can be configured with UVW_DIR and UVW_CPR. Figure 32 shows the options.

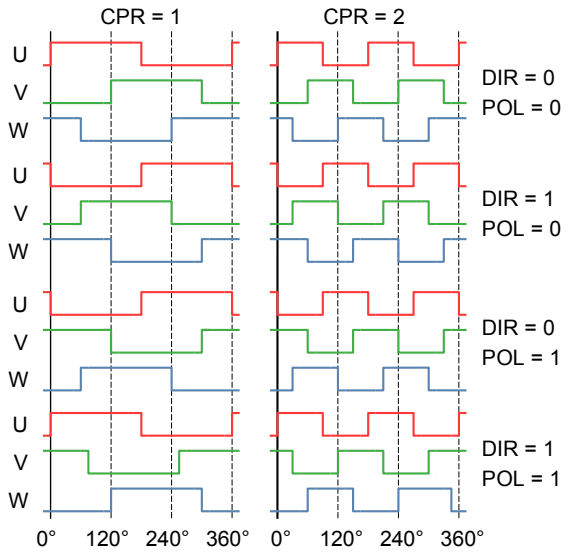

Figure 32: UVW Direction and Polarity

UVW_DIR	Bank 0x7, Addr. 0x01, bit 0	Reset: 0
Code	Function	
0	Rotary direction normal	
1	Rotary direction reversed	

Table 82: UVW Rotary Direction

UVW_POL	Bank 0x7, Addr. 0x01, bit 1	Reset: 0
Code	Function	
0	Normal	
1	Inverted	

Table 83: UVW Polarity

UVW Hysteresis

The iC-NQE avoids loss of motor torque by using a special UVW hysteresis that keeps the UVW edges free from systematic errors as long as the motor direction is not reversed. However, a single edge may be subject to a small hysteresis of 0.7° after a change in direction. As explained in Figure 33, the UVW transition that occurs within 0.7° of a reversal point is shifted by the hysteresis, which reduces the phase of two consecutive transitions by a maximum of 0.7°, but only once.

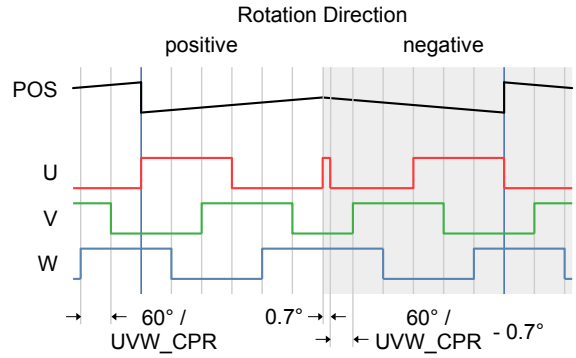

Figure 33: UVW Hysteresis

UVW Position Offset and Latency Compensation

UVW_OFFS adjusts the commutation angle of the motor and is added to the internal angle before UVW generation.

UVW_OFFS(7:0)	Bank 0x7, Addr. 0x02, bit 7:0	Reset: 0x00
UVW_OFFS(15:8)	Bank 0x7, Addr. 0x03, bit 7:0	Reset: 0x00
UVW_OFFS(23:16)	Bank 0x7, Addr. 0x04, bit 7:0	Reset: 0x00
Code	Value	
0x000000	0	
...	*Code*	
0xFFFFFF	$2^{24} - 1$	

Table 84: UVW Output Phase Shift

In addition, a dynamic offset can be programmed with UVW_LTC, which allows to compensate a constant latency in the system. A speed-dependent UVW angle error with respect to the actual motor shaft angle can be avoided in this way, so that no torque losses occur.

UVW_LTC(7:0)	Bank 0x7, Addr. 0x05, bit 7:0	Reset: 0x00
UVW_LTC(15:8)	Bank 0x7, Addr. 0x06, bit 7:0	Reset: 0x00
Code	Value	
0x0000	0 µs	
...	$\frac{3.356}{2^{30}} * Code$	
0x9C39	125 µs	
Others	Not permitted	

Table 85: UVW Latency Compensation

PWM GENERATOR

If the PWM generator is activated via EN_PWM, iC-NQE provides a pulse-width modulated signal at the Z output corresponding to the interpolated angle POS_IA.

EN_PWM	Bank 0x2, Addr. 0x01, bit 6	Reset: 0
Code	Function	
0	PWM generator disabled	
1	PWM generator enabled	

Table 86: PWM Output Enable

The PWM output frequency is about 1 kHz (see Elec.Char. No. B01 on page 14).

At the index position the duty cycle is exactly 50 %, the angular sides to the left and right of it run to 10 % and to 90 %, respectively. If the interpolated angle is not available, the PWM output shows low (no pulse) to indicate an error (see Figure 34).

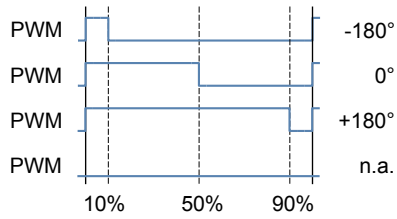

Figure 34: Pulse-width modulated output

MEMORY ORGANISATION

The memory of the iC-NQE is organized in banks. Table 87 shows an overview.

Bank	Address	Content	Location	Access
Registers (Bank n)				
0x00	0x00..0x0F	Test	On-chip RAM	RPL_B0
0x01	0x00..0x0F	OTP	On-chip RAM	RPL_B1
0x02	0x00..0x0F	Interface	On-chip RAM	RPL_B2
0x03	0x00..0x0F	Signal Conditioning and Monitor	On-chip RAM	RPL_B3
0x04	0x00..0x0F	Converter Function and Filter	On-chip RAM	RPL_B4
0x05	0x00..0x0F	Period counter and ADI	On-chip RAM	RPL_B5
0x06	0x00..0x0F	ABZ FlexCount	On-chip RAM	RPL_B6
0x07	0x00..0x0F	UVW FlexCount	On-chip RAM	RPL_B7
0x08	0x00..0x0F	Position Offset	On-chip RAM	RPL_B7
0x09	0x00..0x0F	Register Protection	On-chip RAM	RPL_B8
0x0A..0x0F	0x00..0x3F	Unused		NA
0x10..0x1F	0x00..0x3F	iCAL Data	On-chip RAM	RPL_B16_31
0x20	0x00..0x3F	Other Device Configuration	EEPROM: 0x000..0x03F	RPL_B32
0x21	0x00..0x3F	Direct Access Content	EEPROM: 0x040..0x07F	RPL_B33
0x22..0x23	0x00..0x3F	iC-NQE Device Configuration	EEPROM: 0x080..0x0FF	RPL_B34..RPL_B35
0x24..0x2F	0x00..0x3F	EDS, User Data	EEPROM: 0x100..0x3FF	RPL_B36..RPL_B47
0x30..0x3F	0x00..0x3F	iCAL storage or user data	EEPROM: 0x400..0x7FF	RPL_B48..RPL_B63
0x40..0x43	0x00..0x3F	I2C device 0 data	I2C device memory	RPL_DEV0
0x44..0x47	0x00..0x3F	I2C device 1 data	I2C device memory	RPL_DEV1
0x48..0x4B	0x00..0x3F	I2C device 2 data	I2C device memory	RPL_DEV2
0x4C..0x4F	0x00..0x3F	I2C device 3 data	I2C device memory	RPL_DEV3
Direct Access				
all	0x40	Bank selection	On-chip RAM	RW
all	0x41..0x43	EDS-Bank, Profile ID (DC1) EDS-Bank, Profile ID (DC2) EDS-Bank, Profile ID (DC3)	EEPROM: 0x041..0x043 EEPROM: 0x051..0x053 EEPROM: 0x061..0x063	R R R
all	0x44..0x47	Serial number	EEPROM: 0x044..0x047	R
all	0x48..0x4E	Preset	EEPROM: 0x048..0x04E	RPL_PRES
all	0x50..0x55	Position	On-chip RAM	R
all	0x58..0x5A	Angular velocity	On-chip RAM	R
all	0x60..0x61	Angular acceleration	On-chip RAM	R
all	0x64..0x65	Temperature	On-chip RAM	R
all	0x68..0x6B	Status Flags	On-chip RAM	R
all	0x6C..0x6F	Errors Flags	On-chip RAM	R
all	0x70..0x73	Warnings Flags	On-chip RAM	R
all	0x74..0x75	GPIO	On-chip RAM	RW
all	0x76	Command Register Status	On-chip RAM	R
all	0x77	Command Register	On-chip RAM	RW
all	0x78..0x7D	Device ID (DC1) Device ID (DC2) Device ID (DC3)	EEPROM: 0x078..0x07D EEPROM: 0x058..0x05D EEPROM: 0x068..0x06D	R R R
all	0x7E..0x7F	Manufacturer ID	EEPROM: 0x07E..0x07F	R

Table 87: Memory Organization Overview

Bank Selection
An access to the on-chip memory of iC-NQE (RAM) or the connected devices can be done via any serial I/O interface (see following sections).

All registers are organized via banks. The registers for the chip configuration (RAM) are located on banks 0x00...0x09, and the correction data for linearization of the converter (iCAL in RAM) on banks 0x10...0x1F.

Banks 0x20...0x3F are provided for accesses to the external registers of an EEPROM. Of these, bank 0x20 is intended for the configuration of additional devices.

The banks 0x24...0x2F are available to store an EDS and user data. Additionally, data of up to four external I2C devices can be accessed via banks 0x40...0x4F.

The desired memory bank must be selected in advance with BSEL which sets the *active bank* for access at 0x00 to 0x3F. The bank selector BSEL is located at address 0x40, within the Direct Access registers (range 0x40...0x7F) which are not further subdivided and are directly addressed without regard to the active bank. There are two independent bank selectors, one for I/O interface I^2C and one for BiSS/SPI. Thus two different banks can be active simultaneously, depending on the used interface.

BSEL(7:0)	Addr. 0x40, bit 7:0	Reset: 0x00
Code	Function	
0x00 ...0x4F Others	 Selected Bank Not permitted	

Table 88: Bank selection

Register Protection Level (RPL)
The banks containing the device configuration, the EDS and the user data can be individually protected against write and/or read access. A Register Protection Level (RPL) with states is defined for this purpose:

Code	Function
NA	No access is allowed
RO	Read only
RX	Read and write allowed, but for writing the bank must be opened with the command RPL_SET_RW
RW	Read and write allowed

Table 89: RPL Coding

Changing an RPL is only possible via a RPL_SET_* command. For example, if RX is used to protect a bank against accidental changes, the RPL_SET_RW command must be executed to open the active bank before writing is allowed.

To check the RPL configuration for the active bank, the command RPL_GET can be executed. Note that the RPL settings must be written to the EEPROM to take effect permanently.

In addition, access to I2C devices and execution of the PRESET command can be restricted.

RPL_DEV0(1:0)	Bank 0x9, Addr. 0x09, bit 1:0	Reset: 0x3
RPL_DEV1(1:0)	Bank 0x9, Addr. 0x09, bit 3:2	Reset: 0x3
RPL_DEV2(1:0)	Bank 0x9, Addr. 0x09, bit 5:4	Reset: 0x3
RPL_DEV3(1:0)	Bank 0x9, Addr. 0x09, bit 7:6	Reset: 0x3
Code	Function	
0x0	NA	
0x1	RO	
0x2	RX	
0x3	RW	

Table 90: Register Protection of I^2C devices

RPL_PRES(1:0)	Bank 0x9, Addr. 0x00, bit 5:4	Reset: 0x3
Code	Function	
0x0	NA	
0x1	RO	
0x2	RX	
0x3	RW	

Table 91: Register Protection of Preset

The RPL settings of the configuration banks are stored in the respective bank.

RPL_B2(1:0)	Bank 0x2, Addr. 0x0E, bit 7:6	Reset: 0x3
RPL_B3(1:0)	Bank 0x3, Addr. 0x0E, bit 7:6	Reset: 0x3
RPL_B4(1:0)	Bank 0x4, Addr. 0x0C, bit 7:6	Reset: 0x3
RPL_B5(1:0)	Bank 0x5, Addr. 0x07, bit 7:6	Reset: 0x3
RPL_B6(1:0)	Bank 0x6, Addr. 0x08, bit 7:6	Reset: 0x3
RPL_B7(1:0)	Bank 0x7, Addr. 0x07, bit 7:6	Reset: 0x3
RPL_B8(1:0)	Bank 0x8, Addr. 0x06, bit 7:6	Reset: 0x3
RPL_B9(1:0)	Bank 0x9, Addr. 0x0D, bit 7:6	Reset: 0x3
Code	Function	Description
0x0	NA	No access is allowed
0x1	RO	Read only
0x2	RX	Read and write allowed, but the bank must be opened with command RPL_SET_RW prior writing
0x3	RW	Read and write allowed
Notes	Once the RPL is stored in the EEPROM, it can not be removed anymore.	

Table 92: Register Protection of Configuration Banks

For any other bank that is in external memory, the RPL settings are stored together in bank 0x9.

RPL_B0(1:0)	Bank 0x9, Addr. 0x00, bit 1:0	Reset: 0x3
RPL_B16_31(1:0)	Bank 0x9, Addr. 0x00, bit 3:2	Reset: 0x3
RPL_B32(1:0)	Bank 0x9, Addr. 0x01, bit 1:0	Reset: 0x3
RPL_B33(1:0)	Bank 0x9, Addr. 0x01, bit 3:2	Reset: 0x3
RPL_B34(1:0)	Bank 0x9, Addr. 0x01, bit 5:4	Reset: 0x1
RPL_B35(1:0)	Bank 0x9, Addr. 0x01, bit 7:6	Reset: 0x1
RPL_B36(1:0)	Bank 0x9, Addr. 0x02, bit 1:0	Reset: 0x3
RPL_B37(1:0)	Bank 0x9, Addr. 0x02, bit 3:2	Reset: 0x3
RPL_B38(1:0)	Bank 0x9, Addr. 0x02, bit 5:4	Reset: 0x3
RPL_B39(1:0)	Bank 0x9, Addr. 0x02, bit 7:6	Reset: 0x3
RPL_B40(1:0)	Bank 0x9, Addr. 0x03, bit 1:0	Reset: 0x3
RPL_B41(1:0)	Bank 0x9, Addr. 0x03, bit 3:2	Reset: 0x3
RPL_B42(1:0)	Bank 0x9, Addr. 0x03, bit 5:4	Reset: 0x3
RPL_B43(1:0)	Bank 0x9, Addr. 0x03, bit 7:6	Reset: 0x3
RPL_B44(1:0)	Bank 0x9, Addr. 0x04, bit 1:0	Reset: 0x3
RPL_B45(1:0)	Bank 0x9, Addr. 0x04, bit 3:2	Reset: 0x3
RPL_B46(1:0)	Bank 0x9, Addr. 0x04, bit 5:4	Reset: 0x3
RPL_B47(1:0)	Bank 0x9, Addr. 0x04, bit 7:6	Reset: 0x3
RPL_B48(1:0)	Bank 0x9, Addr. 0x05, bit 1:0	Reset: 0x3
RPL_B49(1:0)	Bank 0x9, Addr. 0x05, bit 3:2	Reset: 0x3
RPL_B50(1:0)	Bank 0x9, Addr. 0x05, bit 5:4	Reset: 0x3
RPL_B51(1:0)	Bank 0x9, Addr. 0x05, bit 7:6	Reset: 0x3
RPL_B52(1:0)	Bank 0x9, Addr. 0x06, bit 1:0	Reset: 0x3
RPL_B53(1:0)	Bank 0x9, Addr. 0x06, bit 3:2	Reset: 0x3
RPL_B54(1:0)	Bank 0x9, Addr. 0x06, bit 5:4	Reset: 0x3
RPL_B55(1:0)	Bank 0x9, Addr. 0x06, bit 7:6	Reset: 0x3
RPL_B56(1:0)	Bank 0x9, Addr. 0x07, bit 1:0	Reset: 0x3
RPL_B57(1:0)	Bank 0x9, Addr. 0x07, bit 3:2	Reset: 0x3
RPL_B58(1:0)	Bank 0x9, Addr. 0x07, bit 5:4	Reset: 0x3
RPL_B59(1:0)	Bank 0x9, Addr. 0x07, bit 7:6	Reset: 0x3
RPL_B60(1:0)	Bank 0x9, Addr. 0x08, bit 1:0	Reset: 0x3
RPL_B61(1:0)	Bank 0x9, Addr. 0x08, bit 3:2	Reset: 0x3
RPL_B62(1:0)	Bank 0x9, Addr. 0x08, bit 5:4	Reset: 0x3
RPL_B63(1:0)	Bank 0x9, Addr. 0x08, bit 7:6	Reset: 0x3

Code	Function
0x0	NA
0x1	RO
0x2	RX
0x3	RW
Notes	The banks 34 and 35 contains configuration data and also, if iCAL is enabled with ICAL_EN = 1, the banks 48..63 contain calibration data and should protected accordingly to prohibit a backdoor access.

Table 93: Register Protection remaining Banks

If backdoor access to configuration data is desired, the RPL_BDOR parameter can be set to unlock banks 34 and 35 independently of their RPL settings.

RPL_BDOR	Bank 0x9, Addr. 0x00, bit 7	Reset: 1
Code	Function	
0	Closed	
1	Opened	

Table 94: RPL Backdoor Enable

Cyclic Redundancy Check (CRC)

The iC-NQE configuration data is secured by an 8-bit CRC for each bank in the respective bank.

CRC Key Parameters	
Parameter	Value
Memory Size	16 bytes (x 8 banks plus OTP)
Gen. Polynomial	$X^8 + X^4 + X^3 + X^2 + X^0$
Characteristic	Hamming distance 3
Error Detection	Up to 2 bits
Start Value	0x30 + bank number

Table 95: CRC of Configuration Data

CRC_B2(7:0)	Bank 0x2, Addr. 0x0F, bit 7:0	Read only
CRC_B3(7:0)	Bank 0x3, Addr. 0x0F, bit 7:0	Read only
CRC_B4(7:0)	Bank 0x4, Addr. 0x0D, bit 7:0	Read only
CRC_B5(7:0)	Bank 0x5, Addr. 0x08, bit 7:0	Read only
CRC_B6(7:0)	Bank 0x6, Addr. 0x09, bit 7:0	Read only
CRC_B7(7:0)	Bank 0x7, Addr. 0x08, bit 7:0	Read only
CRC_B8(7:0)	Bank 0x8, Addr. 0x07, bit 7:0	Read only
CRC_B9(7:0)	Bank 0x9, Addr. 0x0E, bit 7:0	Read only
Code	Function	
All	Checksum	

Table 96: Checksum Configuration Data

The distortion correction data (iCAL) is separately secured by a 16-bit CRC stored under the configuration data in bank 0x9. Changes to the correction data therefore additionally requires an update of the CRC for bank 0x09.

CRC Key Parameters	
Parameter	Value
Memory Size	1024 bytes (on 16 banks)
Gen. Polynomial	$X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + X^0$
Characteristic	Hamming distance 3
Error Detection	Up to 2 bits
Start Value	0x0130

Table 97: CRC of Correction Data (iCAL)

CRC_ICAL(7:0)	Bank 0x9, Addr. 0x0B, bit 7:0	Reset: 0x00
CRC_ICAL(15:8)	Bank 0x9, Addr. 0x0C, bit 7:0	Reset: 0x00
Code	Function	
All	Checksum	

Table 98: Checksum iCAL

OTP

The iC-NQE features a one-time programmable memory (OTP) for the Chip Serial Number SERNO, calibration and tuning data, which is factory programmed by iC-Haus in production. The contents can be read via bank 1.

SERNO(7:0)	Bank 0x1, Addr. 0x00, bit 7:0	Reset: 0x00
SERNO(15:8)	Bank 0x1, Addr. 0x01, bit 7:0	Reset: 0x00
SERNO(23:16)	Bank 0x1, Addr. 0x02, bit 7:0	Reset: 0x00
SERNO(31:24)	Bank 0x1, Addr. 0x03, bit 7:0	Reset: 0x00
Code	Function	
All	Chip Serial Number	

Table 99: Chip Serial Number

EEPROM Access

iC-NQE uses the external EEPROM to store the device configuration non-volatile. The addressing and the data exchange with the external memory is completely taken over by iC-NQE, if a corresponding command is received via one of the serial interfaces.

Either a single bank or the entire device configuration can be read or written. When transferring the configuration data from the on-chip RAM to the EEPROM, the RPL is also stored and the necessary CRC is automatically calculated.

. Refer to COMMAND EXECUTION on page 73 for details.

After power on, the configuration data and the CRC value are read bank by bank. The data of a bank is used if the CRC value confirms correctness, otherwise the bank is re-read up to three times. If this does not succeed, the registers are set to reset values.

When accessing EDS or user data via an address in the corresponding bank, this data is immediately read and written to the EEPROM. Because I2C is used for communication between iC-NQE and the EEPROM, data transfer takes some time to complete.

The corresponding address, which is accessed in the EEPROM, results from the following calculation:

$$EEPROM\_ADR = (BSEL - 0x20) * 0x40 + ADR$$

BISS DEVICE INFO AND EDS

Selected parameters of the Electronic Data Sheet (EDS, from the EEPROM) are mapped into the direct access area (addresses 0x41...0x7F) to facilitate readout. However, writing of these contents is only possible via bank 0x21.

EDS_BANK(7:0)	Addr. 0x41, bit 7:0	Read only
EDS_BANK_2(7:0)	Addr. 0x41, bit 7:0	Read only
EDS_BANK_3(7:0)	Addr. 0x41, bit 7:0	Read only
Code	Function	
0x24 ...0x2F	EDS Bank	
Others	Not permitted	
Notes	This register exists three times, corresponding to the number of individual BiSS-SCD channels.	

Table 100: EDS bank (Channels 1 to 3)

BP_ID(15:8)	Addr. 0x42, bit 7:0	Read only
BP_ID(7:0)	Addr. 0x43, bit 7:0	Read only
BP_ID_2(15:8)	Addr. 0x42, bit 7:0	Read only
BP_ID_2(7:0)	Addr. 0x43, bit 7:0	Read only
BP_ID_3(15:8)	Addr. 0x42, bit 7:0	Read only
BP_ID_3(7:0)	Addr. 0x43, bit 7:0	Read only
Code	Function	
All	BiSS Profile ID	
Notes	This register exists three times, corresponding to the number of individual BiSS-SCD channels.	

Table 101: BiSS Profile ID (Channels 1 to 3)

DEV_SN(31:24)	Addr. 0x44, bit 7:0	Read only
DEV_SN(23:16)	Addr. 0x45, bit 7:0	Read only
DEV_SN(15:8)	Addr. 0x46, bit 7:0	Read only
DEV_SN(7:0)	Addr. 0x47, bit 7:0	Read only
Code	Function	
All	Device Serial Number	

Table 102: Device Serial number

DEV_ID(47:40)	Addr. 0x78, bit 7:0	Read only
DEV_ID(39:32)	Addr. 0x79, bit 7:0	Read only
DEV_ID(31:24)	Addr. 0x7A, bit 7:0	Read only
DEV_ID(23:16)	Addr. 0x7B, bit 7:0	Read only
DEV_ID(15:8)	Addr. 0x7C, bit 7:0	Read only
DEV_ID(7:0)	Addr. 0x7D, bit 7:0	Read only
Code	Function	
All	Identifier	
Notes	This register exists three times, corresponding to the number of individual BiSS-SCD channels.	

Table 103: Device ID (Channels 1 to 3)

MFR_ID(15:8)	Addr. 0x7E, bit 7:0	Read only
MFR_ID(7:0)	Addr. 0x7F, bit 7:0	Read only
Code	Function	
All	Manufacturer ID	

Table 104: Manufacturer ID

I/O INTERFACE BiSS

The BiSS Interface is an open-source interface for bidirectional serial communication with sensors and actuators, which enables the fast transmission of absolute position data with a permanent parameter exchange of status and configuration data. For a detailed description of the BiSS Interface, please refer to www.biss-interface.com.

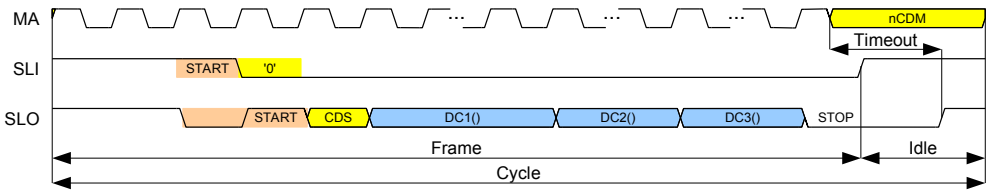

Figure 35: BiSS Transmission

The serial interface is configured for the BiSS-C protocol by setting EN_BISS = 1 and BISS_VER = BiSS-C.

EN_BISS	Bank 0x2, Addr. 0x01, bit 0	Reset: 1
Code	Function	
0	BiSS Interface disabled	
1	BiSS Interface enabled	

Table 105: BiSS Interface Enable

BISS_VER(1:0)	Bank 0x2, Addr. 0x09, bit 1:0	Reset: 0x0
Code	Function	
0x0	BiSS-C	
0x1	BiSS-B	
0x2	SSI	
0x3	Not permitted	

Table 106: BiSS Protocol Variant

In point-to-point connection, a single iC-NQE connects the BiSS Master via the pins MAI and SLO, while pin SLI remains grounded. In bus connection, multiple iC-NQEs form a daisy chain, with SLO feeding the SLI input of the next device. To ensure correct data transmission at high clock rates in bus configuration, the clock output MAO should be activated and wired to the MAI of the subsequent slave.

EN_MAO	Bank 0x2, Addr. 0x01, bit 4	Reset: 0
Code	Function	
0	Output MAO disabled	
1	Output MAO enabled	

Table 107: BiSS Clock Output Enable

Table 108 summarizes the BiSS slave performances that match the biss profiles in all respects. Other configurations are possible for backward compatibility to the iC-NQC, but are not recommended for new designs.

BiSS Slave Performance		
Parameter	Symbol	Description
Clock Rate	$1 / t_C$	Refer to Item No. I001 on page 17
Process.T.	t_{busy}	Refer to Item No. I010 on page 17
Timeout	t_{out}	Refer to Item No. C03 on page 14
SCD Channel 1: Position Data		
Bits/cycle	ID	Description
0..32	POS_PCR	Period Counter (right-aligned) Length according to DL_PCR(2:0).
1..16	POS_IA	Angle Position (left-aligned) Length according to DL_IA(3:0).
1	nE [1]	Error bit ERR
1	nW [1]	Warning bit WARN
(6)	LC	Sign-of-life Counter according to CRC_LC(1:0).
6 (16)	CRC [2]	Polynomial 0x43 (0x190D9), adjustable start value.
SCD Channel 2: Angular Velocity		
Bits/cycle	ID	Description
24	Omega	Angular Velocity
3	UVW	Commutation signals
1	UVW_OK	Commutation Signals valid
1	nE [1]	Error bit ERR
1	nW [1]	Warning bit WARN
6	CRC [2]	Polynomial 0x43, start value zero
SCD Channel 3: Universal		
Bits/cycle	ID	Description
10, 16	UNI	Universal usage
1	nE [1]	Error bit ERR
1	nW [1]	Warning bit WARN
5	CRC [2]	Polynomial 0x25, start value zero
CD Channel: Control Data		
Bits/cycle	ID	Description
1	nCDM [1], CDS	Support of bidirectional register access
	Slave IDs	1 . . . 3
	Commands	Support of selected BiSS Commands according to Table 118.
Notes	[1] Low active. [2] Bit inverted transmission.	

Table 108: BiSS Profile Compliant Slave Performance

Single-Cycle Data (SCD)
The BiSS slave from iC-NQE features up to three single-cycle data (SCD) channels that can be individually selected.

BISS_DC1	Bank 0x2, Addr. 0x0A, bit 4	Reset: 0
Code	Function	
0	Position	
1	Off	

Table 109: BiSS Configuration of Data Channel 1

The **data channel SCD1** transmits the position data, starting with the optional Period Counter (POS_PCR) followed by the Angle Position (POS_IA), the low-active status bits for error (nE) and warning (nW), an optional sign-of-life counter (LC) and the checksum (CRC).

Figure 36: Content of SCD1

The data length of the interpolated angle and the period counter is set by DL_IA and DL_PCR.

DL_IA(3:0)	Bank 0x2, Addr. 0x0B, bit 3:0	Reset: 0x0
Code	Value	
0x0	16	
...	16 – *Code*	
0xF	1	

Table 110: Interpolated Angle Data Length

DL_PCR(5:0)	Bank 0x2, Addr. 0x08, bit 5:0	Reset: 0x00
Code	Value	
0x00	0	
...	*Code*	
0x20	32	
Others	Not permitted	

Table 111: Period Counter Data Length

Data transmission via BiSS is protected by a CRC. The recommended CRC lengths are 6 bits for standard applications (for a Hamming Distance (HD) of 3) and 16 bits for safety applications (for HD of 6). Together with the 16-bit CRC, the transmission of a 6-bit sign-of-life counter (LC) is possible (see CRC_LC). The LC is initialized with 1 and counts up to 63, skipping 0 when wrapping. The counter is incremented with each BiSS frame. The CRC is calculated with the start value specified by CRC_INIT and the CRC bits are transmitted inverted.

CRC_LC(1:0)	Bank 0x2, Addr. 0x0C, bit 1:0	Reset: 0x1
Code	Function	
0x0	5 bit (polynomial 0x25)	
0x1	6 bit (polynomial 0x43)	
0x2	16 bit (polynomial 0x0x190D9)	
0x3	16 bit (polynomial 0x0x190D9) + LC	

Table 112: CRC Length and Sign-of-Life Counter

CRC_INIT(5:0)	Bank 0x2, Addr. 0x0C, bit 7:2	Reset: 0x00
Code	Function	
All	Start value for CRC calculation	

Table 113: CRC Start Value

The **data channel SCD2** transmits the angular velocity (omega) together with the commutation signals (UVW). The channel can be activated with BISS_DC2.

BISS_DC2	Bank 0x2, Addr. 0x0A, bit 5	Reset: 0
Code	Function	
0	Off	
1	Omega	

Table 114: BiSS Configuration of Data Channel 2

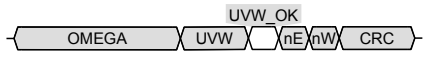

Figure 37: Content of SCD2

A third **data channel SCD3** can be enabled with BISS_DC3.

BISS_DC3(1:0)	Bank 0x2, Addr. 0x0A, bit 7:6	Reset: 0x0
Code	Function	
0x0	Off	
0x1	Reserved	
0x2	Temp	
0x3	not permitted	

Table 115: BiSS Configuration of Data Channel 3

SCD3 is a universal data channel and can transmit the angular acceleration (Alpha) or temperature data. The output format is shown in Figure 37.

Figure 38: Content of SCD3

Timeout
The iC-NQE offers fixed and adaptive timeouts, which are selected via BISS_TOS. The adaptive timeout allows shorter communication cycles and is therefore recommended.

BISS_TOS(1:0)	Bank 0x2, Addr. 0x0A, bit 1:0	Reset: 0x3
Code	Value	
0x0	20 µs	
0x1	128 µs	
0x2	1.5 µs	
0x3	t_{TOA} adaptive	

Table 116: BiSS Timeout

The nominal values of the static timeout depend on the chip's oscillator frequency fosc (see Elec. Char. item no. C03 for tolerances).

If BISS_TOS = 0x3, iC-NQE adjusts its timeout according to the clock period introduced at MAI (see T_{MAI}, Elec. Char. item no. C04). For this purpose, the clock at MAI is evaluated over 1.5 cycles in each BiSS frame, from the first falling edge to the second rising edge, and a value for the adaptive timeout t_{TOA} is calculated from this.

Timeout	Condition	Min.	Max.
t_{TOA}	$T_{CLK} \leq 1.5 * T_{MAI}$	$1.5 * T_{MAI}$	$1.5 * T_{MAI} + 3.0 * T_{CLK}$
	$T_{CLK} \geq 1.5 * T_{MAI}$	$1.0 * T_{CLK}$	$1.5 * T_{MAI} + 3.0 * T_{CLK}$

Table 117: Adaptive timeout calculation

Herein, T_{CLK} is the internal sampling interval derived from fosc (see Elec. Char. item no. 101).

$$T_{CLK} = \frac{4}{3 * fosc}$$

Note: For additional information on the adaptive timeout of BiSS, refer to the BiSS application note AN23 at www.biss-interface.com.

Note: Data output via the BiSS interface is only activated if the CRC check has been passed. It may be necessary to execute the CRC_CALC and CRC_CHECK commands (see section COMMAND EXECUTION on page 73).

Register Communication

In accordance with the BiSS C protocol, iC-NQE basically divides its registers into blocks of 64 bytes, which are either selected dynamically via banks (address range 0x00 to 0x3F) or addressed directly (address range 0x40 to 0x7F).
The memory block that can be reached dynamically under 0x00 to 0x3F is preset by the bank selection BSEL(7:0), which alters the physical memory address. The chapter MEMORY ORGANISATION on page 51 provides information on memory allocation and addressing through BiSS.

BiSS Protocol Commands

The following BiSS interface protocol commands are implemented.

CD Channel: BiSS Commands	
CMD	Function
Addressed	
00	Activate Single-Cycle Data channels
01	Deactivate control communication
10	Not available
11	Not available
Broadcast (all slaves)	
00	Deactivate Single-Cycle Data
01	Activate control communication
10	Reserved
11	Reserved

Table 118: BiSS Protocol Commands

Backward Compatibility to iC-NQC

The following parameters complete the options required to replace the iC-NQC in any application. However, the use of these parameters is not recommended for new designs.

BISS_ZB can add a zero bit between the single-cycle data of iC-NQE and the data of a previous slave read at SLI. STAT_CFG allows to output two error bits instead of error and warning.

BISS_ZB	Bank 0x2, Addr. 0x09, bit 2	Reset: 0
Code	Function	
0	No additional zero bit	
1	One additional zero bit	

Table 119: BiSS Additional Zero Bit Enable

STAT_CFG	Bank 0x2, Addr. 0x09, bit 3	Reset: 0
Code	Function	
0	nE nW	
1	E1 E0	

Table 120: Status Output Configuration

I/O INTERFACE BiSS-B

The serial interface can be configured to the BiSS-B protocol by setting EN_BISS = 1 and BISS_VER = 1.

With BiSS-B the switch to register communication is initiated by a longer timeout at frame start. This register timeout is selectable with BISS_TOR.

BISS_TOR(1:0)	Bank 0x2, Addr. 0x0A, bit 3:2	Reset: 0x0
Code	Value	
0x0	819 µs	
0x1	256 µs	
0x2	32 µs	
0x3	Not permitted	

Table 121: BiSS-B Register Mode Timeout

I/O INTERFACE SSI

The serial interface can be configured to the SSI protocol by setting EN_BISS = 1 and BISS_VER = 2

The interface parameters that define the Single-Cycle Data (SCD) and Timeout for BiSS are also used for SSI, but may not be useful at all. It is also recommended to use a fixed timeout for SSI.

The parameters SSI_GRAY, SSI_RING and SSI_STAT are intended for use with SSI only.

SSI_GRAY	Bank 0x2, Addr. 0x0D, bit 0	Reset: 0
Code	Function	
0	Data is binary coded	
1	Data is Gray coded (status bits are excluded)	

Table 122: SSI Data Format

SSI_RING	Bank 0x2, Addr. 0x0D, bit 1	Reset: 0
Code	Function	
0	SLO stays zero after all bits are clocked out	
1	Data is repeated endlessly, separated by a zero bit	

Table 123: SSI Ring Operation

SSI_STAT	Bank 0x2, Addr. 0x0D, bit 2	Reset: 0
Code	Function	
0	Data output without status bits	
1	Data output with 2 status bits (as defined by STAT_CFG)	

Table 124: SSI Status Output

I/O INTERFACE SPI

The implemented SPI slave (only available with the **QFN package**) supports SPI modes 0 and 3, therefore the idle state of SCLK can be either low or high. Communication is initiated with a falling edge at NCS, which sets iC-NQE active to forward the MOSI signal to MISO and sample data on the rising edge of SCLK.

Each SPI transaction begins with one of the opcodes listed in Table 125, which determine whether configuration (register) or sensor (position) data is accessed. Data is sent byte by byte with the MSB first. Figure 39 shows an example of an SPI transmission.

Opcodes

OPCODE	
Code	Description
0x81	Read Register
0xCF	Write Register
0xA6	Read Position
0x97	Request Data From I2C Slave
0xD2	Transmit Data To I2C Slave
0xAD	Get Transaction Info
0xB0	Activate Slave In Chain

Table 125: SPI Operation Codes

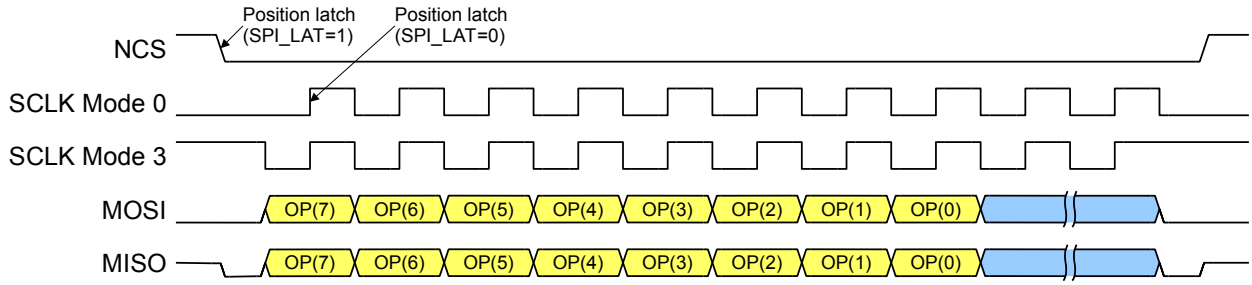

Figure 39: SPI Transmission

The SPI slave is enabled by EN_SPI shares the pins with the BiSS interface (see Table 127 for mapping). The differential pins MAI-NMAI and SLI-NSLI must be configured for single-ended operation (refer to PCFG_MAI and PCFG_SLI).

EN_SPI	Bank 0x2, Addr. 0x01, bit 1	Reset: 1
Code	Function	
0	SPI disabled	
1	SPI enabled	

Table 126: SPI Enable

SPI Pin Mapping	
Pin	Function
NSLI	NCS
MAI	SCLK
SLI	MOSI
SLO	MISO

Table 127: SPI pin mapping

If both interfaces are enabled at the same time (i.e. EN_SPI = 1 and EN_BISS) = 1), the selection is done by the pin NCS. If NCS is high and SPI not selected, the serial interface executes BiSS or SSI depending on BISS_VER. In this case the pin MISO is driven strongly and operates as data output SLO.

Therefore, disabling BiSS (by EN_BISS = 0) is recommended to avoid side effects when using SPI. In addition, when BiSS is disabled, MISO remains in tristate (high Z) when NCS is high, and clock pulses received at SCLK/MAI are ignored. This enables the bussing of multiple iC-NQEs to a single SPI master. For more information, see Bussing and Chaining Multiple iC-NQEs on page 61.

Note: Connecting a pull-up or pull-down resistor to MISO may be required to prevent input floating of chained devices (during NCS high).

Read Registers

Opcode Read Registers (0x81) is used to read data from any number of consecutive registers in the on-chip RAM. As shown in Figure 40, the data stream to be sent on MOSI consists of the opcode 0x81, followed by the address of the first register to be read and a delay byte 0x00. Those first three bytes are also transmitted by iC-NQE on MISO, before sending the requested data (DATA1) from the register at address (ADR). As long as clock is sent and the slave stays active, data

(DATA2) from the next register at the incremented address (ADR + 1) is transmitted. This procedure may be continued for any number of consecutive registers.

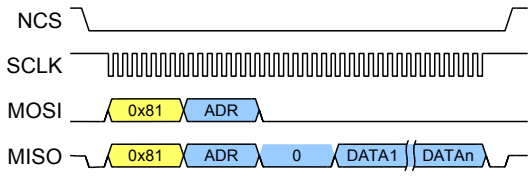

Figure 40: Read Register

Write Registers

Opcode Write Registers (0xCF) is used to write data to any number of consecutive registers in the on-chip RAM. As shown in Figure 41, the data stream to be sent on MOSI consists of the opcode 0xCF, followed by the address of the first register to be written and the data. With each data byte the address of the register to be written is incremented by one (ADR + 1). If successfully received, the same data stream is transmitted on MISO by iC-NQE.

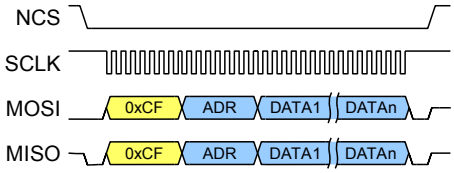

Figure 41: Write Register

Read Position

Opcode Read Position (0xA6) is used to read the absolute position data from iC-NQE (see Figure 42). The position data will be latched either on the first rising edge of SCLK (for SPI_LAT = 0) or on the falling edge of NCS (for SPI_LAT = 1) as shown previously in Figure 39.

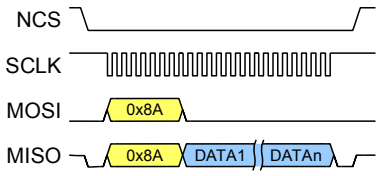

Figure 42: Read Position

SPI_LAT	Bank 0x2, Addr. 0x0D, bit 4	Reset: 0
Code	Function	
0	SCLK	
1	NCS	

Table 128: Data Trigger Source for SPI

As shown in Table 129, the position data format consists of the period counter followed by the angle position, an error bit, a warning bit, an optional sign-of-life counter (LC) and a CRC value. While the angle position is always 16 bits, the period counter is adjustable in length with DL_PCR(2:0)).

Read Position Format	
Byte Length	Description
for CRC_LC(1:0) < 3	
0 . . . 4	Period Counter (according to DL_PCR(2:0))
2	Angle Position
1	nERR, nWARN, 6-bit CRC
for CRC_LC(1:0) = 3	
0 . . . 4	Period Counter (according to DL_PCR(2:0))
2	Angle Position
1	nERR, nWARN, 6-bit LC
2	16-bit CRC
Note	Period and angle data includes the offsets adjusted via PCR_OFFS and IA_OFFS.

Table 129: SPI Read Position Format

The position information is transmitted in one of two data formats as shown in Table 129, selected via CRC_LC(1:0) as shown in Table 130.

The first format (CRC_LC(1:0) < 3) includes one low-active error bit, one low-active warning bit and a 6-bit CRC.
The second format (CRC_LC(1:0) = 3) includes one low-active error bit, one low-active warning bit, a 6-bit sign-of-life counter (LC) and a 16-bit CRC. The LC counts from 1 to 63 skipping the 0 when wrapping and is incremented with each SPI Read Position frame.

CRC_LC(1:0)	Bank 0x2, Addr. 0x0C, bit 1:0	Reset: 0x0
Code	CRC HEX Code	Description
0x00 0x01 0x02	0x43	6-bit CRC polynomial: $X^6 + X^1 + X^0$ Hamming Distance: 3 Max data length: 57 bits No sign-of-life counter is transmitted
0x03	0x190D9	16-bit CRC polynomial: $X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + X^0$ Hamming Distance: 6 Max data length: 64 bits A 6-bit sign-of-life counter is transmitted. The counter starts at 0 counting from 1 to 63 and omitting 0 when wrapping.

Table 130: Sign-of-Life Counter and CRC for SPI

Note that the total data length is limited to either 57 or 64 bits (counted without the CRC bits). The CRC is calculated with the start value defined by CRC_INIT and its value transmitted in its inverted state at the end of each SPI frame.

Request Data From I2C Slave

Data from external devices connected to the I2C master of iC-NQE (e. g. EEPROM) can be requested via opcode Request Data From I2C Slave (0x97). As shown in Figure 43, the opcode followed by the register address of the I2C slave has to be sent on MOSI. The same content is transmitted by iC-NQE on MISO. After the opcode has been received, the initiated I2C communication will take additional time until completed. Opcode Get Transaction Info is used to poll for the current I2C communication status and new data.

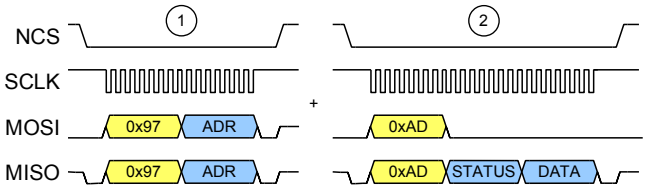

Figure 43: Request Data From I2C Slave

Transmit Data To I2C Slave

Data to external devices connected to the I2C master of iC-NQE (e. g. EEPROM) can be transmitted via opcode Transmit Data To I2C Slave (0xD2). As shown in Figure 44, the opcode followed by the register address of the I2C slave and the data byte to be transmitted has to be sent on MOSI. The same content is transmitted by iC-NQE on MISO. After the opcode has been received, the initiated I2C communication will take additional time until completed. Opcode Get Transaction Info is used to poll for the current I2C communication status.

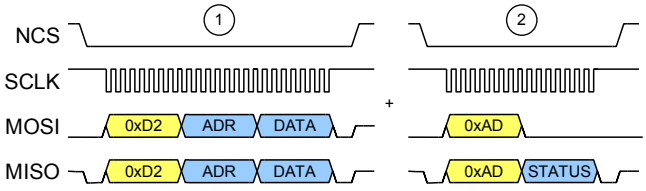

Figure 44: Transmit Data To I2C Slave

Get Transaction Info

Via opcode Get Transaction Info (0xAD) the status of the last initiated SPI transaction is returned. Opcodes Read Position (0xA6) and Get Transaction Info (0xAD) itself are not updating the status byte. As shown in Figure 45, only the opcode has to be sent on MOSI. The opcode followed by the status byte defined in Table 131 is transmitted by iC-NQE on MISO. The data byte is only defined, if opcode Request Data From I2C Slave has been sent before.

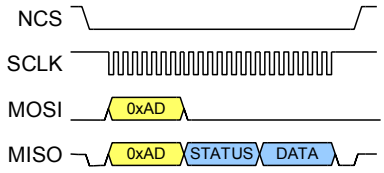

Figure 45: Get Transaction Info

STATUS		
Bit	Name	Description
7	Error	Invalid opcode
6:4	-	Reserved
3	Dismiss	Illegal Address
2	Fail	Data request failed
1	Busy	Slave busy
0	Valid	Data valid

Table 131: SPI Status Byte

If an error occurs during a register read access (invalid address, invalid data, etc.), the Fail bit in the SPI status byte is set and the data returned is invalid. If an error occurs during a register write access (invalid address, invalid data, etc.), the Fail bit in the SPI Status byte is set and the data in not written. In both error cases, the address counter is no longer incremented.

Note that the opcode Get Transaction Info may return data from a previous transaction if the foregoing opcode Request Data From I2C Slave has not yet completed.

Multi-Slave Configurations with iC-NQE

A common SPI bus configuration for two iC-NQE is illustrated in Figure 46. Each slave is selected individually by the SPI master via a dedicated NCS line. Only one slave may communicate at the same time.

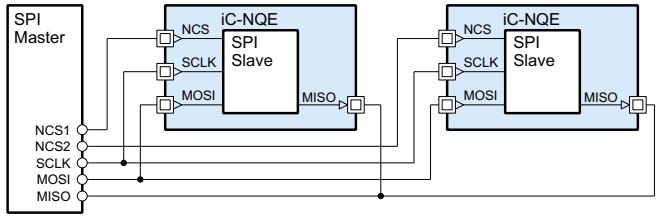

Figure 46: SPI bus configuration

Another possibility to connect multiple iC-NQE is by setting up an SPI daisy chain as shown in Figure 47. The MISO of each iC-NQE is connected to the MOSI of the next device. As only a single NCS line is used, indi-

vidual slaves are selected via opcode Activate Slave in Chain.

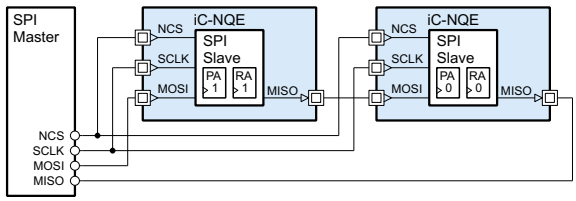

Figure 47: SPI daisy chain configuration

Note: Reading the current state of RACTIVE and PACTIVE is not possible. If the status is lost, the SPI master must turn off both channels and then activate each or both as required with the Activate command.

Activate Slave In Chain

Each iC-NQE provides two separate channels for register and position data transfer that can be switched on and off individually. Register communication with iC-NQE is only possible if RACTIVE = 1. Otherwise register communication attempts are ignored. Position data can only be acquired from iC-NQE if PACTIVE = 1. Otherwise opcode Read Position (0xA6) is ignored.

By sending opcode Activate Slave in Chain (0xB0) each iC-NQE acts as a 2-bit shift register containing one RACTIVE and one PACTIVE configuration bit. RACTIVE and PACTIVE bits are initialized as '0', turning both data channels off. The SPI Status Byte is reset (i.e. Fail, Valid, Busy, and Dismiss bits are all reset).

Following the opcode (0xB0), the desired RACTIVE/-PACTIVE channel configuration is transmitted. Data bytes corresponding to all possible configurations are shown in Table 134. Slave number 0 is considered to be the last slave in chain directly connected to MISO of the SPI master.

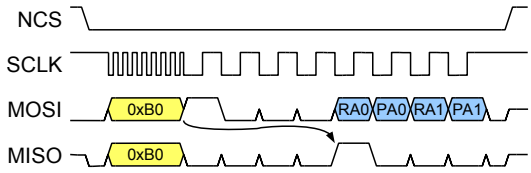

Figure 48: Activate Command for two slaves

RACTIVE	default: 1
Code	Description
0	Register communication deactivated
1	Register communication activated

Table 132: RACTIVE

PACTIVE	default: 1
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated

Table 133: PACTIVE

iC-NQE enables both data channels after startup to support SPI in point-to-point connection (RACTIVE = 1, and PACTIVE = 1).

Slaves	**RA/PA configuration byte 0**								**RA/PA configuration byte 1**							
2	0	0	0	0	RA0	PA0	RA1	PA1	Not used							
3	0	0	RA0	PA	RA1	PA1	RA2	PA2	Not used							
4	RA0	PA0	RA1	PA1	RA2	PA2	RA3	PA3	Not used							
5	0	0	0	0	0	0	RA0	PA0	RA1	PA1	RA2	PA2	RA3	PA3	RA4	PA4
6	0	0	0	0	RA0	PA0	RA1	PA1	RA2	PA2	RA3	PA3	RA4	PA4	RA5	PA5
7	0	0	RA0	PA0	RA1	PA1	RA2	PA2	RA3	PA3	RA4	PA4	RA5	PA5	RA6	PA6
8	RA0	PA0	RA1	PA1	RA2	PA2	RA3	PA3	RA4	PA4	RA5	PA5	RA6	PA6	RA7	PA7

Table 134: RA/PA channel configuration bits for 2-8 slaves

I/O INTERFACE I2C

The implemented I²C interface includes a multi-master capable controller for accessing connected I²C slave devices (e.g. EEPROM), as well as a slave interface that can be accessed by an external master controller:

- The built-in I²C master (controller) restores the chip configuration from an external EEPROM at power on (see section STARTUP and OPERATION on page 28). During regular operation, communication with any connected I²C slaves (e.g. temperature sensors) can be initiated via BiSS (or SPI if available).
- The I²C slave (target) interface can be used by an external master (controller) to configure the iC-NQE at power on, as well as to monitor and manipulate parameters during operation using the BiSS interface (or SPI if available). It is also possible to set BSEL for SPI/BiSS writing to 0x41 using the I²C slave.

The I²C transmission is shown in Figure 49, the implemented features in Table 135. If required, additional I²C descriptions are offered by NXP, see I²C-bus specification and user manual.

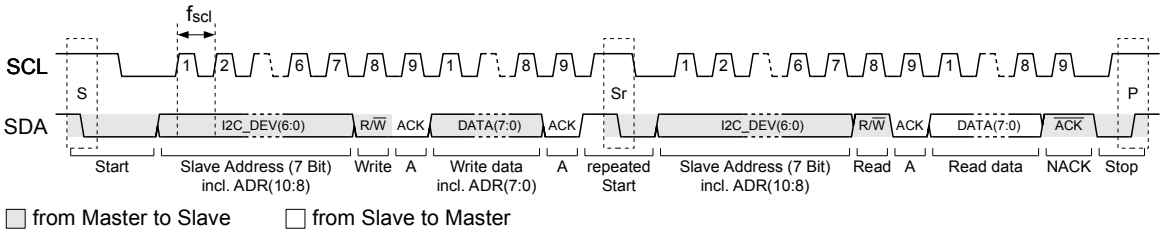

Figure 49: Combined I²C write/read command accessing a single slave register.

I²C Performance		
	Multi-Master	Slave
Protocol	Fast-mode	Fast-mode
START Condition	Mandatory	Mandatory
STOP Condition	Mandatory	Mandatory
Acknowledge	Mandatory	Mandatory
Synchronization	Mandatory	n/a
Arbitration	Mandatory	n/a
Clock Stretching	Implemented	n/a
7-bit Target Address	Mandatory	Mandatory
10-bit Target Address	Not available	Not available
General Call Address	Available	Available
Soft Reset	Not available	Not available
START Byte	Not available	n/a
Device ID	n/a	Not available
Bus Clear	Available	n/a
Clock Rate	350 kHz typ. (refer to Elec.Char. E01	400 kHz max.

Table 135: I²C Interface Performance

I²C Master to EEPROM

A conventional EEPROM features a slave address with a group number on the highest four bits (A = 1010), followed by three lower bits extending the address pointer byte. The total number of 11 address bits allows to access memory of up to 16 Kbit maximum. Accordingly, the iC-NQE uses a two byte addressing for serial EEPROMs, such as 24C01 to 24C16.

EEPROM Device Requirements	
Supply Voltage	3.0 V to 5.5 V (according to VDD)
Power-On Threshold	< 2.8 V (due to Elec.Char. 207)
Addressing	11 bit address max.
Device Address	0x50 (’1010 000’ w/o R/W bit), 0xA0 (’1010 0000’ with R/W = 0)
Page Buffer	Not required
Size Min. (for configuration w/o ICAL_EN)	2 Kbit (256x8 bit), type 24C02
Size Min. (for configuration with ICAL_EN)	16 Kbit (8x 256x8 bit), type 24C16
Size Max.	16 Kbit (8x 256x8 bit), type 24C16 Size limited due to 11-bit slave addressing.

Table 136: EEPROM Device Requirements

Figure 49 shows a typical example of communication. The first byte send after the start condition contains the slave address with the R/W bit for the data direction. The I²C master executes a write access with R/W = 0 first, to transmit an address pointer of 1 byte to the slave. Second, a read access with R/W = 1 is executed, in which the slave returns the register content (here of 1 byte) according to the preset address pointer.

Auxiliary Device Addressing

Besides the EEPROM, iC-NQE can access another four I²C devices, for which the I2C_DEV0 to I2C_DEV3 registers provide the target addresses.

I2C_DEV0(6:0)	Bank 0x2, Addr. 0x03, bit 6:0	Reset: 0x00
I2C_DEV1(6:0)	Bank 0x2, Addr. 0x04, bit 6:0	Reset: 0x00
I2C_DEV2(6:0)	Bank 0x2, Addr. 0x05, bit 6:0	Reset: 0x00
I2C_DEV3(6:0)	Bank 0x2, Addr. 0x06, bit 6:0	Reset: 0x00

Code	Function
0x00 ...0x4F	Slave address of external I²C devices
0x50 ...0x57	Not allowed (occupied by I²C EEPROM)
0x58 ...0x7F	Slave address of external I²C devices

Table 137: I2C Target Addresses

A maximum of 256 bytes per slave can be handled, occupying four register banks of 64 bytes each. Refer to the address mapping of I²C devices (EEPROM and other) in section MEMORY ORGANISATION on page 51.

I²C Slave Interface

An external I²C master (controller) can access the iC-NQE by its slave interface via the slave address 0x64.

Single Read

Reading any desired address is executed in a combined cycle with a write access, to first set the internal address pointer on the slave, and then a read access, to transmit the desired data subsequently.

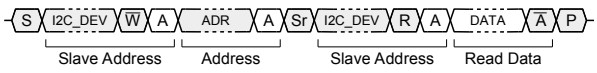

Figure 50: Combined Format For Reading

Current Address Read

If the I²C slave does not feature an internal address pointer or if the pointer was already set, the read access can be executed without a previous write access.

Figure 51: Reading From Current Address

Sequential Read

Since the internal address pointer of common I²C slaves is incremented automatically (after the initial acknowledge), the iC-NQE supports the consecutive reading of registers by continued cycles. Finally, when the last byte has been reached, iC-NQE inverts the acknowledge bit (NACK).

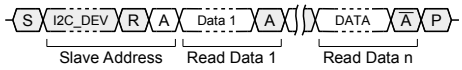

Figure 52: Sequential Reading

Note: Current Address Read and Sequential Read is not implemented in Revision 0.

Single Write

Writing to any I²C slave register is executed in one cycle with setting the address pointer prior to writing data.

Figure 53: Random Writing

Sequential Page Write

A sequential write to the I²C slave is possible under restriction. Since the EEPROM takes time for programming and only a limited data volume can be buffered, the iC-NQE can be configured with I2C_PAGE for compliance to the page size being available.

I2C_PAGE(1:0)	Bank 0x2, Addr. 0x07, bit 1:0	Reset: 0x0

Code	Value
0x0	1 Byte
0x1	4 Byte
0x2	8 Byte
0x3	16 Byte

Table 138: I2C Mode Page Size Configuration

The iC-NQE supports the consecutive writing of registers by continued cycles as shown in Figure 54, up to the byte count configured with I2C_PAGE.

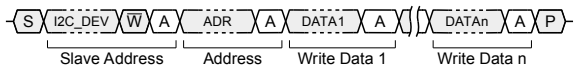

Figure 54: Sequential Writing

Acknowledge Polling

Writing data to the EEPROM may require multiple access cycles when not using page write, or when exceeding the page size. As long as the EEPROM is not ready for communication, the iC-NQE master repeats the addressing until the acknowledge signal is received. The repetition phase can last about 35 ms before a communication error is recognized.

Figure 55: Acknowledge Polling

Bus Clear
If the data line (SDA) is stuck at low, the iC-NQE outputs nine clock pulses. If SDA is held low for longer, an error code will be filed.

Error Handling
I²C interface errors are stored to I2C_ERC at address 0x6E. The error code is maintained only until a reset or power cycle.

I2C_ERC(2:0)	Addr. 0x6E, bit 6:4	Read only
Code	Function	
0x0	No error	
0x1	SCL stuck at 0	
0x2	SDA stuck at 0	
0x3	Acknowledge polling timeout	
0x4	Unexpected error	
0x5	Arbitration loss	

Table 139: I2C Error Code

OUTPUT DATA

The IC's measurement data (period count, angle position, angular velocity, and temperature) is available as Single-Cycle Data (SCD1...SCD3) via BiSS and SSI. Using SPI, the Read Position command provides the period counter and angle position. In both cases the output data is big-endian formatted.

Besides, the direct access memory is available to any serial I/O Interface. In this case, the output data is little-endian formatted according to the chip's internal register arrangement (see Table 2, section Output Data). For data occupying several addresses, the first access to the base address ensures storage of the entire data word, up to the most significant byte, so that consistent data can be read subsequently. For example, reading address 0x58 returns OMEGA(7:0) but also saves OMEGA(23:16) for subsequent accesses.

POS_IA(7:0)	Addr. 0x50, bit 7:0	Read only
POS_IA(15:8)	Addr. 0x51, bit 7:0	Read only
Code	Function	
Unsigned	Interpolated angle (lower part of position, 16 bit)	

Table 140: Angle Position Data

POS_PCR(7:0)	Addr. 0x52, bit 7:0	Read only
POS_PCR(15:8)	Addr. 0x53, bit 7:0	Read only
POS_PCR(23:16)	Addr. 0x54, bit 7:0	Read only
POS_PCR(31:24)	Addr. 0x55, bit 7:0	Read only
Code	Function	
Unsigned	Period counter (higher part of position, 32 bit)	

Table 141: Period Counter Data

OMEGA(7:0)	Addr. 0x58, bit 7:0	Read only
OMEGA(15:8)	Addr. 0x59, bit 7:0	Read only
OMEGA(23:16)	Addr. 0x5A, bit 7:0	Read only
Code	Value	
0x000000	0 rad/s	
...	+1.8722 rad/s∗*Code*	
0x7FFFFF	+15705355 rad/s	
0x800000	−15705357 rad/s	
...	−1.8722 rad/s∗(0x*FFFFFF* − *Code* + 1)	
0xFFFFFF	−1.8722 rad/s	
Notes	[1] Calculated with fosc = 80 MHz (Refer to Electrical Characteristics, Item No. 101 on page 10)	

Table 142: Angular Velocity of PSIN, NSIN, PCOS, NCOS

Position Offset and Counting Direction

The output position can be shifted by adding offsets to the interpolated angle (via IA_OFFS) and to the period count (via PCR_OFFS). The configuration of these registers is taken over by iC-NQE when the command PRESET is executed. Thereby the target position can be zero or individually configured.

IA_OFFS(7:0)	Bank 0x8, Addr. 0x00, bit 7:0	Reset: 0x00
IA_OFFS(15:8)	Bank 0x8, Addr. 0x01, bit 7:0	Reset: 0x00
Code	Function	
Unsigned	Offset for interpolated angle	

Table 143: Interpolated Angle Offset

PCR_OFFS(7:0)	Bank 0x8, Addr. 0x02, bit 7:0	Reset: 0x00
PCR_OFFS(15:8)	Bank 0x8, Addr. 0x03, bit 7:0	Reset: 0x00
PCR_OFFS(23:16)	Bank 0x8, Addr. 0x04, bit 7:0	Reset: 0x00
PCR_OFFS(31:24)	Bank 0x8, Addr. 0x05, bit 7:0	Reset: 0x00
Code	Function	
Unsigned	Offset for period counter	

Table 144: Period Counter Offset

It is possible to reverse the data direction for the serial I/O interfaces with DIR. The setting has no effect on the ABZ or UVW output.

DIR	Bank 0x4, Addr. 0x04, bit 6	Reset: 0
Code	Function	
0	Code direction normal	
1	Code direction reversed	

Table 145: Position Counting Direction

DIAGNOSTIC FUNCTIONS

Status Flags

The status flag registers at addresses 0x68 to 0x6B provide information about current comparator values and general system states. They refer to the state diagram in Figure 13 of section STARTUP and OPERATION.

SUPPLY	Addr. 0x69, bit 4:0	Read only
Bit	Name	Description
Logic Supply monitoring flags: 0 = NOK, 1 = OK		
0	VDDA_OK	Voltage at VDDA
1	VDD_OK	Voltage at VDD
Logic Voltage domain flags: 0 = 3.3 V, 1 = 5 V		
2	VDDA_DOM	Voltage domain at VDDA
3	VDD_DOM	Voltage domain at VDD
Logic level at pin NERR: 0 = NOK, 1 = OK, Pin is released (not forced low)		
4	NERR_I	Voltage at I/O pin NERR

Table 146: Supply Monitoring Flags

RDY	Addr. 0x68, bit 5:0	Read only
Bit	Name	Description
Logic Ready flags: 0 = Event has not occurred 1 = Event has occurred		
0	RDY_CFG	Configuration phase finished
1	RDY_PCR	Period counter initialized
2	RDY_PHI	Interpolated angle settled
3	RDY_ABZ	AB Output initialized and running
4	RDY_UVW	UVW Output initialized and running
5	RDY_CMD	Command execution finished

Table 147: Ready Flags

AMP_*	Addr. 0x6A, bit 5:0		Read only
Bit	Name	Function	Threshold
0	AMP_G_L	Gain Control [1]	Vpp()minG
1	AMP_G_H	Gain Control [2]	Vpp()maxG
2	AMP_W_L	Warning [1]	Vpp()minW
3	AMP_W_H	Warning [2]	Vpp()maxW
4	AMP_E_L	Error [1]	Vpp()minE
5	AMP_E_H	Error [2]	Vpp()maxE
[1] Lo-Comparator	0 = Not OK (poor level, gain to low) **1 = OK** (amplitude above minimum threshold)		
[2] Hi-Comparator	**0 = OK** (amplitude below maximum threshold) 1 = Not OK (excessive level, gain to high)		

Table 148: Signal Monitoring Flags

GC_ERR_L	Addr. 0x6B, bit 6	Read only
GC_ERR_H	Addr. 0x6B, bit 7	Read only
Code	Function	
0	Control limit not reached	
1	Control limit reached	

Table 149: Gain Control Status

ABS_OK	Addr. 0x68, bit 6	Read only
UVW_OK	Addr. 0x68, bit 7	Read only
ZERO_OCC	Addr. 0x6B, bit 5	Read only
Bit	Name	Description
Logic: 0 = Referencing pending, 1 = Referencing occurred		
6	ABS_OK	Absolute position valid (ZERO occurred)
7	UVW_OK	Commutation position valid (ZERO occurred)
5	ZERO_OCC	First ZERO occurred (referencing completed)

Table 150: Position Valid Status

STATE(4:0)	Addr. 0x6B, bit 4:0	Read only
Code	Function	
0x00	PowerOn	
0x01 ...0x03	ReadOtp	
0x04 ...0x0A	ReadE2Prom	
0x0B	ConfigError	
0x0C	SoftReset	
0x0D	CalculateOutput	
0x0E	Operate	
0x0F ...0x11	CheckCRC	
0x12 ...0x14	CalculateCRC	
0x15 ...0x1B	WriteConfigToE2Prom	
0x1C ...0x1F	PresetSequence	

Table 151: Execution Status

Error Flags

The error flag registers at addresses 0x6C to 0x6E indicate internal and external events according to the following table.

ERR(7:0)	Addr. 0x6C, bit 7:0	Read only
ERR(15:8)	Addr. 0x6D, bit 7:0	Read only
ERR(17:16)	Addr. 0x6F, bit 1:0	Read only
Bit	Name	Description
Logic: 0 = No Error, 1 = Error is active		
0	ERR_ADI	ADI Summary Error
1	ERR_IA_F	IA Filter Error
2	ERR_OMEG	IA Velocity Error
3	ERR_ALPH	IA Acceleration Error
4	ERR_ABZ	ABZ Flexcount Error
5	ERR_UVW	UVW Flexcount Error
6	ERR_IA_C	IA Carryover Error
7	ERR_FERR	Excessive Frequency Error
8	ERR_AMPL	Low Level Error
9	ERR_AMPH	High Level Error
10	ERR_AMPM	Minimum Level Error
11	ERR_I2C	I2C Summary Error
12	ERR_EXT	External Error
13	ERR_WD	Watchdog Error
14	ERR_CFG	Configuration Error
15	ERR_FLAG	Error Message Flag
16	ERR_VDDA	VDDA Supply Monitor Error
17	ERR_VDD	VDD Supply Monitor Error
	Notes	IA = Interpolated Angle

Table 152: Error Flag

ERR_MASK(7:0)	Bank 0x4, Addr. 0x08, bit 7:0	Reset: 0x00
ERR_MASK(14:8)	Bank 0x4, Addr. 0x09, bit 6:0	Reset: 0x00
Bit	Name	Description
Logic: 0 = Not selected, 1 = Selected		
0	EM_ADI	ADI Summary Error Mask
1	EM_IA_F	IA Filter Error Mask
2	EM_OMEGA	IA Velocity Error Mask
3	EM_ALPHA	IA Acceleration Error Mask
4	EM_ABZ	ABZ Flexcount Error Mask
5	EM_UVW	UVW Flexcount Error Mask
6	EM_IA_C	IA Carryover Error Mask
7	EM_FERR	Excessive Frequency Error Mask
8	EM_AMPL	Low Level Error Mask
9	EM_AMPH	High Level Error Mask
10	EM_AMPM	Minimum Level Error Mask
11	EM_I2C	I2C Summary Error Mask
12	EM_EXT	External Error Mask
13	EM_VDDA	VDDA Supply Monitor Error Mask
14	EM_VDD	VDD Supply Monitor Error Mask

Table 153: Error Mask

The corresponding masking register controls the error visibility for the serial I/O interface and the NERR pin.

Error events can be latched until clearing action with ERR_LAT.

ERR_LAT	Bank 0x4, Addr. 0x09, bit 7	Reset: 0
Code	Function	
0	Error flag is not latched	
1	Error flag is latched until cleared with SCLEAR	

Table 154: Error Latch Enable

When using the Absolute Data Interface (ADI), the error displayed on ERR_ADI can be verified using the following ADI error flags.

ADI_FRM(1:0)	Addr. 0x6E, bit 3:2	Read only
Code	Function	
0x0	No error	
0x1	ADA/=1 at startup	
0x2	ADI/=0 at timeout	
0x3	Invalid configuration	

Table 155: ADI Frame Error

ADI_PCR	Addr. 0x6E, bit 1	Read only
Code	Function	
0	No error	
1	PCR comparison failed	

Table 156: ADI-PCR Comparison Failed

ADI_EB	Addr. 0x6E, bit 0	Read only
Code	Function	
0	No error	
1	Error bit received	

Table 157: ADI Error Bit Received

I²C interface errors are stored to I2C_ERC.

I2C_ERC(2:0)	Addr. 0x6E, bit 6:4	Read only
Code	Function	
0x0	No error	
0x1	SCL stuck at 0	
0x2	SDA stuck at 0	
0x3	Acknowledge polling timeout	
0x4	Unexpected error	
0x5	Arbitration loss	

Table 158: I2C Error Code

Warning Flags

The warning flag registers at addresses 0x70 to 0x71 indicate internal and external events according to the following table. The corresponding masking register controls the warning visibility for the serial I/O interface only. Warning events can be latched until clearing action with WRN_LAT.

WRN(7:0)	Addr. 0x70, bit 7:0	Read only
WRN(15:8)	Addr. 0x71, bit 7:0	Read only
WRN(17:16)	Addr. 0x73, bit 1:0	Read only
Bit	Name	Description
Logic: 0 = No Warning, 1 = Warning is active		
0	WRN_ADI	ADI WB received or Sync. limit reached
1	WRN_IA_F	IA Filter Warning
2	WRN_OMEG	IA Velocity Warning
3	WRN_ALPH	IA Acceleration Warning
4	WRN_ABZ	ABZ Flexcount Warning
5	WRN_UVW	UVW Flexcount Warning
6	WRN_IA_C	IA Carryover Warning
7	WRN_FERR	Excessive Frequency Warning
8	WRN_AMPL	Low Level Warning
9	WRN_AMPH	High Level Warning
15	WRN_FLAG	Warning Message Flag
16	WRN_VDDA	VDDA Supply Monitor Warning
17	WRN_VDD	VDD Supply Monitor Warning

Table 159: Warning Flag

WRN_MASK(7:0)	Bank 0x4, Addr. 0x0A, bit 7:0	Reset: 0x00
WRN_MASK(14:8)	Bank 0x4, Addr. 0x0B, bit 6:0	Reset: 0x00
Bit	Name	Description
Logic: 0 = Not selected, 1 = Selected		
0	WM_ADI	ADI Warning Bit Mask
1	WM_IA_F	IA Filter Warning Mask
2	WM_OMEGA	IA Velocity Warning Mask
3	WM_ALPHA	IA Acceleration Warning Mask
4	WM_ABZ	ABZ Flexcount Warning Mask
5	WM_UVW	UVW Flexcount Warning Mask
6	WM_IA_C	IA Carryover Warning Mask
7	WM_FERR	Excessive Frequency Warning Mask
8	WM_AMPL	Low Level Warning Mask
9	WM_AMPH	High Level Warning Mask
13	WM_VDDA	VDDA Supply Monitor Warning Mask
14	WM_VDD	VDD Supply Monitor Warning Mask

Table 160: Warning Mask

WRN_LAT	Bank 0x4, Addr. 0x0B, bit 7	Reset: 0
Code	Function	
0	Warning flag is not latched	
1	Warning flag is latched until cleared with SCLEAR	

Table 161: Warning Latch Enable

TEMPERATURE SENSOR

The iC-NQE provides an on-chip temperature sensor, which can be enabled by EN_TEMP. The temperature value is stored in TEMP, coded in signed 2's complement format. This register is read only. Refer to Elec. Char. No. 802 on page 13 for the temperature range covered.

EN_TEMP	Bank 0x2, Addr. 0x02, bit 1	Reset: 0
Code	Function	
0	Temperature sensor disabled	
1	Temperature sensor enabled	

Table 162: Temperature Sensor Enable

TEMP(7:0)	Addr. 0x64, bit 7:0	Read only
TEMP(15:8)	Addr. 0x65, bit 7:0	Read only
Code	Function	
Signed (2K)	$\frac{\text{Code}}{10}\,^{\circ}\text{C}$	

Table 163: Temperature Data

GPIO

iC-NQE provides up to eight GPIO pins that can act as general purpose input/output. The GPIO function is always active as fallback solution if no other output function determines the pin function (see I/O INTERFACE DRIVERS / RECEIVERS).

The GPIO pin function, input or output, is selected by GPIO_D. For an enabled pin driver GPIO_F determines the pin state; optionally a high or low level can be driven. The output state can be read back via GPIO_R.

GPIO_D_0	Addr. 0x74, bit 0	Reset: 0
GPIO_D_1	Addr. 0x74, bit 1	Reset: 0
GPIO_D_2	Addr. 0x74, bit 2	Reset: 0
GPIO_D_3	Addr. 0x74, bit 3	Reset: 0
GPIO_D_4	Addr. 0x74, bit 4	Reset: 0
GPIO_D_5	Addr. 0x74, bit 5	Reset: 0
GPIO_D_6	Addr. 0x74, bit 6	Reset: 0
GPIO_D_7	Addr. 0x74, bit 7	Reset: 0
Code	Function for each pin	
0	Input: Driver disabled	
1	Output: Driver enabled	

Table 164: GPIO Direction

GPIO_F_0	Addr. 0x75, bit 0	Write only
GPIO_F_1	Addr. 0x75, bit 1	Write only
GPIO_F_2	Addr. 0x75, bit 2	Write only
GPIO_F_3	Addr. 0x75, bit 3	Write only
GPIO_F_4	Addr. 0x75, bit 4	Write only
GPIO_F_5	Addr. 0x75, bit 5	Write only
GPIO_F_6	Addr. 0x75, bit 6	Write only
GPIO_F_7	Addr. 0x75, bit 7	Write only
Code	Function	
0	Force low level at GPIOx	
1	Force high level at GPIOx	

Table 165: GPIO Force Value

GPIO_R_0	Addr. 0x75, bit 0	Read only
GPIO_R_1	Addr. 0x75, bit 1	Read only
GPIO_R_2	Addr. 0x75, bit 2	Read only
GPIO_R_3	Addr. 0x75, bit 3	Read only
GPIO_R_4	Addr. 0x75, bit 4	Read only
GPIO_R_5	Addr. 0x75, bit 5	Read only
GPIO_R_6	Addr. 0x75, bit 6	Read only
GPIO_R_7	Addr. 0x75, bit 7	Read only
Code	Function	
0	Low level at GPIOx received	
1	High level at GPIOx received	

Table 166: GPIO Read Value

SIN/COS OUTPUTS

The analog signal path of the iC-NQE operates free of multiplexers and independent of the interpolation engine. According to Figure 15, the conditioned input signals are connected to the embedded cable drivers, which provide the industry standard differential line signal of 1 Vpp for 100 Ω termination (Figure 56) when enabled by EN_ADRV.

EN_ADRV	Bank 0x2, Addr. 0x02, bit 0	Reset: 0
Code	Function	
0	Output driver disabled	
1	Output driver enabled	

Table 167: Output Driver Enable

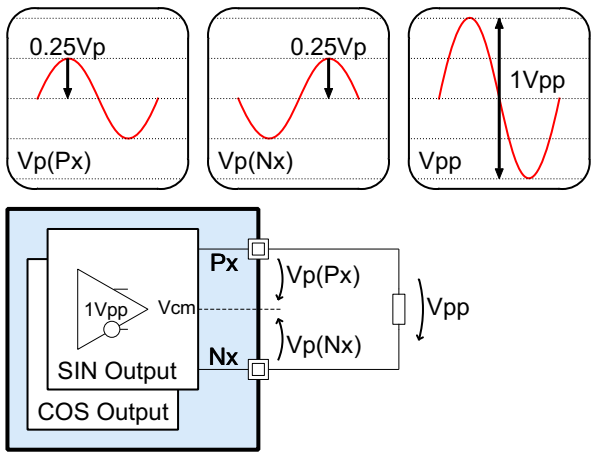

Figure 56: Output Signal Amplitudes

The Sin/Cos outputs are not available in TSSOP20 package.

I/O INTERFACE DRIVERS / RECEIVERS

Interface	Pin Name															
	A	NA	B	NB	Z	NZ	PZERO	NZERO	SLO	NSLO	MA	NMA	SLI	NSLI	SDA	SCL
ABZ	A	NA	B	NB	Z	NZ										
UVW	U	U	V	V	W	W										
		NU		NV		NW										
BiSS					MAO	MAO			SLO	NSLO	MA	NMA	SLI	NSLI		
										MAO						
SPI									MISO		SCLK		MOSI	NCS		
I2C															SDA	SCL
GPIO	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7								
ADI							ACL	ADA								
PWM					PWM											
Comparator							PZERO	NZERO								
Calibration	PCOS		NCOS												PSIN	NSIN

Table 168: Possible pin signals depending on interface configuration.

The iC-NQE has several interfaces that can be mapped to different pins. Possible combinations are listed in Table 168.

Table 169 explains the crossbar configuration of pin A. If e.g. TMA1 is set, pin A provides the signal PCOS. In all other cases pin A provides either A, U or GPIO0 depending on the configuration of EN_ABZ and EN_UVW.

Crossbar Pin A			
TMA1	EN_ABZ	EN_UVW	Pin A
1	x	x	PCOS
0	1	x	A
0	0	1	U
0	0	0	GPIO0

Table 169: Crossbar Pin A

Furthermore, by setting PCFG_A it is possible to choose between single-ended and RS422 mode.

PCFG_SLO	Bank 0x2, Addr. 0x00, bit 4	Reset: 1
PCFG_A	Bank 0x2, Addr. 0x00, bit 5	Reset: 0
PCFG_B	Bank 0x2, Addr. 0x00, bit 6	Reset: 0
PCFG_Z	Bank 0x2, Addr. 0x00, bit 7	Reset: 0
Code	Function	
0	SE	
1	RS422	

Table 170: Pin A, B, Z, SLO Configuration

The output function of pin NA depends on the above selection, see Table 171. For example, if TMA1 is selected for pin A, pin NA changes to tristate.

Otherwise, if TMA1 is not set but PCFG_A is set, pin NA provides the complementary signal to A, i.e. NA, as required for RS422.
If staying on single-ended, pin NA can output U or operate as GPIO1, as shown in Table 171.

Crossbar Pin NA				
TMA1	PCFG_A	EN_ABZ	EN_UVW	Pin NA
1	x	x	x	Tristate
0	1	x	x	Diff to Pin A
0	0	1	1	U
0	0	1	0	GPIO1
0	0	0	x	GPIO1

Table 171: Crossbar Pin NA

The configuration of other pins is very equal to A and NA, see the following Tables.

Crossbar Pin B			
TMA1	EN_ABZ	EN_UVW	Pin B
1	x	x	NCOS
0	1	x	B
0	0	1	V
0	0	0	GPIO2

Table 172: Crossbar Pin B

Crossbar Pin NB				
TMA1	PCFG_B	EN_ABZ	EN_UVW	Pin NB
1	x	x	x	Tristate
0	1	x	x	Diff to Pin B
0	0	1	1	V
0	0	1	0	GPIO3
0	0	0	x	GPIO3

Table 173: Crossbar Pin NB

Crossbar Pin Z				
EN_PWM	EN_ABZ	EN_UVW	EN_MAO	Pin Z
1	x	x	x	PWM
0	1	x	x	Z
0	0	1	x	W
0	0	0	1	MAO
0	0	0	0	GPIO4

Table 174: Crossbar Pin Z

Crossbar Pin NZ					
PCFG_Z	EN_ABZ	EN_UVW	EN_MAO	PCFG_SLO	Pin NZ
1	x	x	x	x	Diff of Pin Z
0	1	1	x	x	W
0	1	0	1	1	MAO
0	0	1	1	1	MAO
0	0	0	x	x	GPIO5

Table 175: Crossbar Pin NZ

Crossbar Pin NSLO		
PCFG_SLO	EN_MAO	Pin NSLO
1	x	Diff to Pad SLO
0	1	MAO
0	0	0

Table 176: Crossbar Pin NSLO

Crossbar Pin SDA & SCL		
TMA1	Pin SDA	Pin SCL
1	PSIN	NSIN
0	SDA	SCL

Table 177: Crossbar Pin SDA & SCL

Crossbar Pin PZERO & NZERO			
EN_ZERO	ADI_EN	Pin PZERO	Pin NZERO
1	x	PZERO	NZERO
0	1	ACL	ADA
0	0	GPIO6	GPIO7

Table 178: Crossbar Pin PZERO & NZERO

Regarding the I/O Interfaces, the output function of SLO changes with the selection of the interface, there is no crossbar to configure. Therefore the only option is to select RS422 with PCFG_SLO.

Further options are available for the receiver inputs, the MAI and SLI pins, for which PCFG_MAI and PCFG_SLI select between differential (RS422) or single-ended input with CMOS or TTL thresholds.

PCFG_MAI(1:0)	Bank 0x2, Addr. 0x00, bit 1:0	Reset: 0x0
PCFG_SLI(1:0)	Bank 0x2, Addr. 0x00, bit 3:2	Reset: 0x0
Code	Function	
0x0	SE-CMOS	
0x1	SE-TTL	
0x2	RS422	
0x3	OFF	

Table 179: Pin MAI, SLI Configuration

COMMAND EXECUTION

The CMD register provides predefined commands that can be called via the serial interface in use. As long as a command is executed, the CMD register keeps the entered value. On successful execution, the CMD register is reset to 0x00; if an error occurs, 0xFF is set.

It is forbidden to send a new command while another command is still being executed. Therefore it is essential to query CMD after calling a command and check for 0x00.

For some commands an additional command status register provides useful information about the execution, which can be interesting in case of an error. For example, CMD_STAT may indicate an access violation if a protection setting would block addressed registers.

CMD_STAT(7:0)	Addr. 0x76; bit 7:0	default: 0x00, Read only
Code	Value	
CRC_CHECK		
n	n = Amount of wrong bank CRCs.	
CONF_WRITE, CONF_WRITE_ALL		
0x00	Ok	
0x50	Illegal bank selected	
0x60	Write not allowed	
RPL_SET_x		
0x00	Ok	
0x50	Illegal bank selected	
0x60	Change refused. Only lower privileges are allowed.	
RPL_GET		
0x00	No-access	
0x01	Read-only	
0x02	Read and write after unlock	
0x03	No restriction	
0x50	Illegal bank selected	
FORCE_x		
0x00	Ok	
0x01	Refused due to RPL_B2.	
0x02	Refused. Interface disabled.	
others		
0x00	No data returned.	

Table 180: Command Status

Preset Function

The preset function calculates new position offset values based on the current position data and the configured target position for both the singleturn data (under PRES_IA) and the multiturn data (under PRES_PCR).

The checksum PRES_CRC is used for verification when reading the external EEPROM.

Note that the period counter preset value may cover part of the singleturn position if more than one sin/cos cycle per revolution is evaluated (for PCR_ML > 1).

The calculated position offset values are stored in IA_OFFS and PCR_OFFS, see section OUTPUT DATA for details.

PRES_IA(7:0)	Addr. 0x48, bit 7:0	Read only
PRES_IA(15:8)	Addr. 0x49, bit 7:0	Read only
Code	Function	
Unsigned	Preset value for interpolated angle	

Table 181: Interpolated Angle Preset

PRES_PCR(7:0)	Addr. 0x4A, bit 7:0	Read only
PRES_PCR(15:8)	Addr. 0x4B, bit 7:0	Read only
PRES_PCR(23:16)	Addr. 0x4C, bit 7:0	Read only
PRES_PCR(31:24)	Addr. 0x4D, bit 7:0	Read only
Code	Function	
Unsigned	Preset value for period counter	

Table 182: Period Counter Preset

PRES_CRC(7:0)	Addr. 0x4E, bit 7:0	Read only
Code	Function	
All	Checksum preset	

Table 183: Checksum Preset

Command Protection

Command usage can be restricted with CPL.

CPL	Bank 0x9, Addr. 0x0A, bit 4:0	Reset: 0x1F
Bit	Name	Description
Logic: 0 = Command is rejected, 1 = Commend is permitted		
0	CPL_F_EW	Command Permit Level (Un)Force Err/Wrn
1	CPL_PRES	Command Permit Level Preset
2	CPL_GPIO	Command Permit Level GPIO
3	CPL_F_IF	Command Permit Level (Un)Force Interfaces
4	CPL_BISS	Command Permit Level BiSS Commands 0 and 1

Table 184: Command Permit Level

The following table shows all implemented commands:

CMD(7:0)		Addr. 0x77; bit 7:0	default: 0x00
Code	Name	Description	
0x00	<NOP_OK>	<Return-code: last operation succeded>	
0xFF	<NOP_FAIL>	<Return-code: last operation failed>	
0x10	REBOOT	Reboot the device equivalent to power-on reset.	
0x11	RESET	Reset the device. Restart using internal config. data	
0x12	STANDBY	Go into Standby-Mode with reduced power consumption.	
0x20	SCLEAR	Clear the status registers.	
0x21	FORCE_ERR	Force the error bit to active.	
0x22	UNFORCE_ERR	Don't force the error bit to active.	
0x23	FORCE_WRN	Force the warning bit to active.	
0x24	UNFORCE_WRN	Don't force the warning bit to active.	
0x30	CRC_CALC	Recalculate and apply valid CRC checksums for all configuration banks.	
0x31	CRC_CHECK	CRC verification of all internal configuration banks.	
0x40	CONF_READ_ALL	Restart and read configuration from OTP and EEPROM.	
0x41	CONF_WRITE_ALL	Write current configuration of all banks to EEPROM.	
0x43	CONF_WRITE	Write current configuration of the active bank [1] to EEPROM.	
0x80	PRESET	Start Preset Sequence.	
0x90	GPIO0_SET0	Set general purpose pin GPIO0 to 0.	
0x91	GPIO0_SET1	Set general purpose pin GPIO0 to 1.	
0x92	GPIO1_SET0	Set general purpose pin GPIO1 to 0.	
0x93	GPIO1_SET1	Set general purpose pin GPIO1 to 1.	
0x94	GPIO2_SET0	Set general purpose pin GPIO2 to 0.	
0x95	GPIO2_SET1	Set general purpose pin GPIO2 to 1.	
0x96	GPIO3_SET0	Set general purpose pin GPIO3 to 0.	
0x97	GPIO3_SET1	Set general purpose pin GPIO3 to 1.	
0x98	GPIO4_SET0	Set general purpose pin GPIO4 to 0.	
0x99	GPIO4_SET1	Set general purpose pin GPIO4 to 1.	
0x9A	GPIO5_SET0	Set general purpose pin GPIO5 to 0.	
0x9B	GPIO5_SET1	Set general purpose pin GPIO5 to 1.	
0x9C	GPIO6_SET0	Set general purpose pin GPIO6 to 0.	
0x9D	GPIO6_SET1	Set general purpose pin GPIO6 to 1.	
0x9E	GPIO7_SET0	Set general purpose pin GPIO7 to 0.	
0x9F	GPIO7_SET1	Set general purpose pin GPIO7 to 1.	
0xA0	RPL_SET_NA	Set the active bank [1] to no-access (read and write protected).	
0xA1	RPL_SET_RO	Set the active bank [1] to read only.	
0xA2	RPL_GET	Get the register protection level of the active bank [1]. The result is stored in CMD_STAT.	
0xA3	RPL_SET_RW	Remove the Read/Write protection from the active bank [1].	
0xA5	RPL_SET_RX	Set the active bank [1] to read and write after unlock.	
0xB0	AC_WRITE	Write adjustment values from automatic calibration to configuration ram.	
0xC0	UNFORCE_IF	Use the default protocol on the multi-function interface.	
0xC1	FORCE_BISS	Force the multi-function interface into BiSS protocol (e.g. to switch from SSI to BiSS) [2].	
0xC2	FORCE_SSI	Switch the multi-function interface to SSI protocol (e.g. to switch from BiSS to SSI, without breaking the control frame register communication) [2].	
0xC3	FORCE_SSIADI	Switch to SSI protocol with the ADI slave as second in chain (e.g. to measure an offset between ADI data and the ST data, without breaking the control frame register communication) [2].	
0xC4	FORCE_SPI	Force the multi-function interface into SPI protocol [2].	
0xE0	CHIP_ID	The 16-bit chip ID is returned in CMD_STAT (low byte first).	
0xE1	CHIP_REV	The chip revision is returned in CMD_STAT.	

[1] The active bank is defined by BSEL and must be programmed via BiSS or SPI (not by I2C).
[2] The FORCE commands overrules the configuration but the RAM content is preserved.

Table 185: Commands

DESIGN REVIEW: Function Notes

iC-NQE Z1		
No.	Function, Parameter/Code	Description and Application Notes
		None at time of release.

Table 186: Notes on chip functions regarding iC-NQE chip release Z1.

REVISION HISTORY

Rel.	Rel. Date†	Chapter	Modification	Page
A2	2025-04-01		Initial release	all

Rel.	Rel. Date†	Chapter	Modification	Page
A3	2025-05-15	SINE-TO-DIGITAL CONVERTER	Table 37: column added for range	40
		ABSOLUTE DATA INTERFACE (ADI)	Figure 27 added on ADI Raw Data Mode	43

† Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-NQE	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant	Temperature range -40 °C to +125 °C	iC-NQE QFN32-5x5
Evaluation Board			iC-NQE EVAL NQ8D
iC-NQE	– Preliminary – 20-pin TSSOP, RoHS compliant Contact iC-Haus for availability.	Temperature range -25 °C to +85 °C.	iC-NQE TSSOP20
Evaluation Board	– Preliminary – Contact iC-Haus for availability.	Contact iC-Haus for availability.	iC-NQE EVAL NQ6D

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